LaserVision ROM disc drive VP415/00/05/35

Service
Service
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LaserVision

42 050 A12

Service Manual

LV ROM

The VP415 is a professional Video Disc Drive for use in computerized audiovisual systems, involving a high degree of interactivity.
The Drive is suitable for playback of pre-recorded optical video discs, according to the LaserVision system (PAL standard) and it has the capacity to handle LV-ROM (LaserVision Read Only Memory) interactive discs.

The differences between /00, /05 and/35 are only related to the ornamental plate on the front panel and to the mainscord.
Version /00 = LV-ROM Disc Drive with Euro mainscord.
/05 = BBC Domesday version with GB mainscord
/35 = /00 with GB mainscord

Contents:

Caution

"Use of controls or adjustments or performance of procedures other than those specified here in may result in hazardous radiation exposure".

Safety regulations require that the set be restored to its original condition and that parts which are identical with those specified be used.

CLASS 1
LASER PRODUCT
3122 110 03420

DocumentationTechnique Service Dokumentation Documentazione di Servizio Huolte-Ohje Manual de Servicio Manual de Serviçio

Subject to modification
GB 4822 726 14282
Printed in The Netherlands

Published by
Service Consumer Electronics

CS 7 814

Chapter 1

Technical data
Controls, indicators, connections
Connector pinning

TECHNICAL DATA

LASERVISION DISC

Disc diameter	30 cm (12") or 20 cm (8")
Disc thickness	2.7 mm (0.1")
Disc speed	CAV disc: 1500 r.p.m. CLV disc: 1500-570 r.p.m.
Maximum capacity (30 cm - 12" disc)	CAV disc: 54000 pictures per side LV-ROM disc (CAV): 324 Mbyte (max.) user data per side (in place of audio)
Max. playingtime	CAV disc: 36 minutes per side CLV disc: 1 hour per side
Average track pitch	1.6-1.8 µm

LASERVISION DISC DRIVE VP415

General

Front loading motor-powered disc-tray

startup time	<13s
unload time (time between Eject command and disc out of player)	<15s
SSL (solid state laser)	
Laser type	AlGaAs semiconductor
Wavelength	780 nm
Aperture	0.5
Output of laser	3 - 5 mW
Random access time	CAV: max. 3s (≤1 s average) CLV: max. 15s (≤5 s average)
Instant jump	up to 50 frames (forward or reverse) within vertical interval time
On-board programming	Up to 16 picture number/chapter number segments
Program retention with no mains supply	at least 1 week
Mains voltage	220-240 V (±10%) a.c.
Mains frequence	50 to 60 Hz
Power consumption	60 W approx.
Electrical safety	acc. to IEC 65
operational conditions	10 to 35 °C
Rel. humidity	20-80%
storage conditions	−40 to 70 °C
Rel. humidity	10-95%
Dimensions	420×160×400mm
disc-tray open	420×160×740mm
Weight	15 kg (approx.)
TV system	625/50 PAL

Video

CVBS input (BNC)	1 V into 75 Ω, loop-through
CVBS output (BNC)	1 V into 75 Ω
CVBS output (Euroconnector pin 19)	1 V into 75 Ω
RGB output (Euroconnector)	
R (pin 15)	0.7 V into 75 Ω
G (pin 11)	0.7 V into 75 Ω
B (pin 7)	0.7 V into 75 Ω
Video bandwidth	RGB: 5 MHz (−3dB) CVBS: 3 MHz (−3 dB), encoded
Signal-to-noise ratio	40 dB typ. unweighted (disc dependent) 50 dB typ. weighted (disc dependent)
Timebase instability	less than 10ns (normal play)

Audio

Audio input (cinch)	3 Vpp (load 47 k)
Audio output (cinch)	650 mV r.m.s. into 1k (max. deviation)
Audio output (Euroconnector pins 1 & 3)	650 mV r.m.s. into 1 k
Audio bandwidth	40-20 000 Hz
Signal-to noise ratio	≥ 50 dB typ. weighted (disc dependent)
Channel separation	better than 55 dB

Genlock

Sync input (BNC)	0.3-2.0 Vpp 75Ω, loop-though (wavefrom acc. to CCIR standards)
Sync input (DIN pin 4)	line freq. 15 625 Hz ± 100 ppm field freq. 50 Hz locked to line freq., interlaced, with or without equalising pulses, negative-going, logic 0:0-1 V, logic 1:2.2-4.2 V
Sync output (BNC)	2.0 Vpp 75 Ω, negative-going
Genlock lock-in time	5s

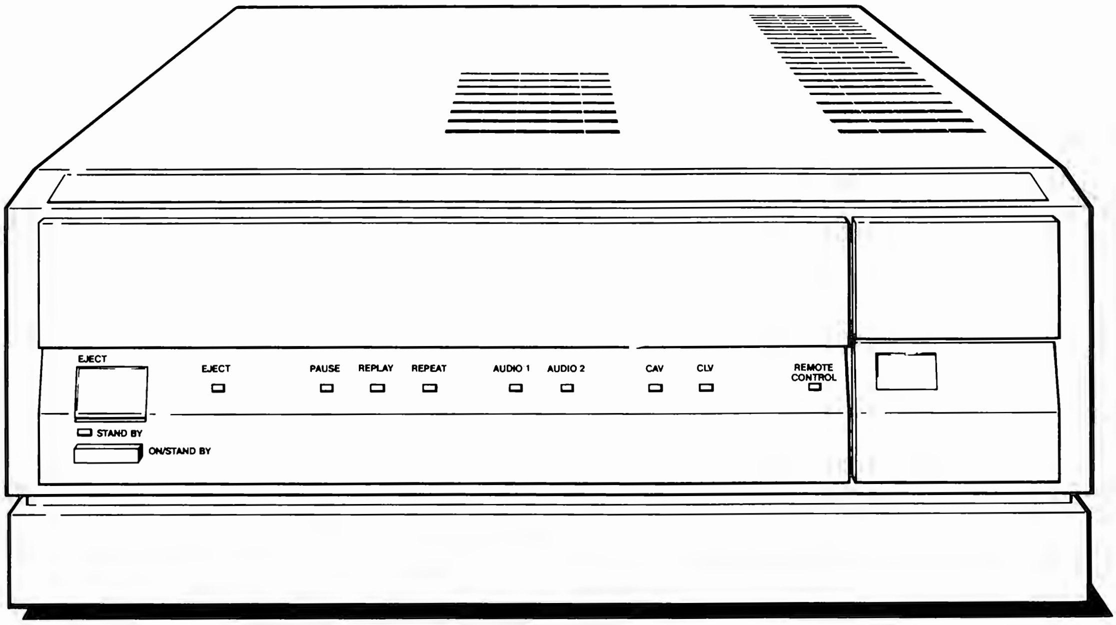
Video mixer

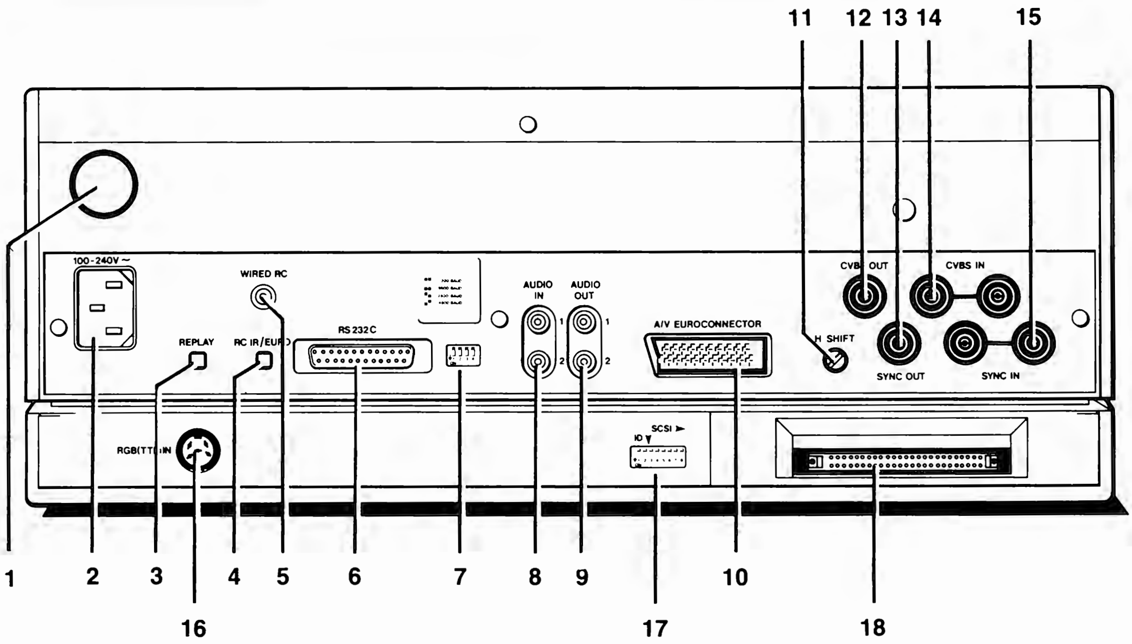
RGB mixing/keying modes:
- Player RGB only
- Computer output RGB only
- Mixed mode: player 62%, computer 38%
- Key mode: player 100%, computer 100%
- Enhanced mode: Player 57%/100%

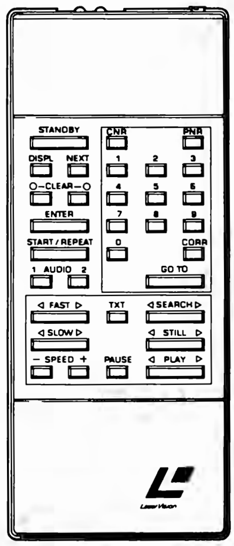
LV-ROM

User data capacity	Max. 324 Mbyte per disc side
User data per frame	6 kbyte
User data transfer rate from disc	150 kbyte/s (depending on computer)
Data integrity (error rate)	$\leq 10^{-16}$
Internal C.P.U.	4X6 kbyte cache memory for user data
System	compatible with floppy disc and hard disc systems

CONTROLS, INDICATORS AND CONNECTIONS







Front

EJECT button
STANDBY indicator
ON/STANDBY button
EJECT indicator
PAUSE indicator
REPLAY indicator
REPEAT indicator
AUDIO 1 indicator
AUDIO 2 indicator
CAV indicator
CLV indicator
REMOTE CONTROL indicator

Rear

1 ON/OFF switch
2 MAINS lead socket
3 REPLAY on/of switch
4 RC IR/EURO switch
5 WIRED RC socket
6 RS232C socket
7 BAUD RATE dip switches
8 AUDIO IN (1&2) sockets
9 AUDIO OUT (1&2) sockets
10 A/V EUROCONNECTOR
11 H-SHIFT control [for Genlock]
12 CVBS OUT socket
13 SYNC OUT socket
14 CVBS IN socket
15 SYNC IN sockets
16 RGB (TTL) IN socket
17 SCSI address dip switches
18 SCSI socket

Remote control functions

- Play forward/reverse
- Still frame/step forward/reverse
- Audio 1/2 on/off
- Picture number/time display on/off
- Chapter number display on/off
- Programme display on/off
- Search forward/reverse (20 times normal speed)
- Goto (Picture or Chapter number)
- Input correction
- Digits 0-9 entry
- Fast forward/reverse (3,10,20 x normal speed)
- Slow forward/reverse (1/100 to normal speed)
- Fast/slow rate +/-
- Clear memory
- Enter
- Standby
- Pause
- Start/Repeat
- Next

A/V Euroconnector

Pin	signal
1	audio out (right) 650 mV rms/1k
2	not connected
3	audio out (left) 650 mV rms/1k
4	audio earth
5	blue earth
6	not connected
7	blue out 700 mV/75 Ω
8	player status (player in standby: 2 V, player on : 12 V)
9	green earth
10	not connected
11	green out 700 mV/75 Ω
12	not connected
13	red earth
14	earth
15	red out 700 mV/75 Ω
16	fast blanking: 2.5 V into 75 Ω (RGB status)
17	CVBS earth
18	RGB status earth
19	CVBS out 1 V/75 Ω (also ects as sync out when using RGB)
20	not connected
21	socket earth

RGB (TTL) IN socket (DIN)
6-pole female connector, 270 degrees

pin	
1	Red signal
2	Green signal
3	Blue signal
4	Composite sync
5	Ground
6	Not connected

(logic 0:0 -1 V, logic 1:2.2. –4.2 V. Sync instability better than +/– 100 pm, interlaced, with or without equalising pulses, negative going.)

RS232-C interface

Serial computer interface, in accordance with international communication standards.
Full duplex
8 data bits, 1 stop bit, no parity

Data transmission speed may be set to 1200/2400/4800/9600 baud according to the positions of the two baud rate dip switches (numbers 1 and 2) at the rear of the player.

Baud rate	switch 1	switch 2
1200	UP	UP
2400	UP	DOWN
4800	DOWN	UP
9600	DOWN	DOWN

The player is fitted with a 25-pole female D-connector with the following pin connections:

pin	signal
2 (TxD)	transmitted data from player to computer
3 (RxD)	received data from computer to player
5 (CTS)	clear to send: a signal from computer to player indicating the computer is ready to receive data (⩾+3 V means O.K. to transmit)
7 (GND)	logic ground
9	+12 V/100 mA
10	–12 V/10 mA
20 (DTR)	data terminal ready: a signal from player to computer indicating that player is ready to receive data (⩾+3 V means O.K. for data)

SCSI interface

A computer interface in accordance with SCSI standards. The player is fitted with a 50-pole unshielded connector consisting of two rows of 25 male pins on 100 mil centres.

Single-ended cable pin assignments:

pin	signal
2	-DB(0)
4	-DB(1)
6	-DB(2)
8	-DB(3)
10	-DB(4)
12	-DB(5)
14	-DB(6)
16	-DB(7)
18	-DB(P)
20	GROUND
22	GROUND
24	GROUND
26	*TERMPWR (**not** connected to internal power supply)
28	GROUND
30	GROUND
32	-ATN
34	GROUND
36	-BSY
38	-ACK
40	-RST
42	-MSG
44	-SEL
46	-C/D
48	-REQ
50	-I/O

Notes

All odd pins except pin 25 are connected to ground. Pin 25 should be left open, but may be connected to ground.

A minus sign indicates active low.

Maximum cable length is 6 m.

•Address dip switches at rear of player. Dip switch in **up** position = OFF. Switches 1-4 and switch 8 should be OFF. Switches 5-7 determine the SCSI bus address of the player as follows:

address	switch 5	switch 6	switch 7
0	OFF	OFF	OFF
1	OFF	OFF	ON
2	OFF	ON	OFF
3	OFF	ON	ON
4	ON	OFF	OFF
5	ON	OFF	ON
6	ON	ON	OFF
7	ON	ON	ON

(Factory setting: address 0)

Termination according to SCSI: 330 Ω TO +5 V
220 Ω to 0 V

If you have more than one device connected to the host computer via the SCSI bus, the SCSI bus termination in the player has to be altered.
For details see* note in diagram of LV-ROM Interface Module Wb.

REMARKS

1. Care of the disc drive

The disc drive requires no special maintenance.
It is, however, recommended to clean the objective lens from time to time with a piece of wadding, dipped in alcohol.

2. Set–up of the Service Manual

The set is composed of various modules (A through Z). The circuit diagrams, PCB layouts and parts lists have also been classified per module.

a) *Circuit diagrams*

Of each module a functional circuit diagram has been given, with the incoming signals drawn as much as possible at the left–hand side and the outgoing signals at the right–hand side. Each incoming and outgoing signal has a unique name, the meaning of which can be read in the Signal listing.
If a signal enters or leaves the module, this takes place via a connector (e.g. 6B2 = pin 6 of connector B2) and via a letter indication in the line. This indication mentions to which module the line is connected.
If the letter indication in the line is the same as the module on which the signal is present, the signal remains on the module mentioned and, naturally, no connector is drawn.

b) *Oscillograms and voltages in the circuit diagrams*

- The oscillograms in the diagrams have been measured with a dual–beam scope with Delayed Timebase PM3214. The set has been connected to a monitor by means of a SCART cable
  Video : still picture, picture number 5530
  (EBU colour bar, 75% saturation)
  Audio 1: normal play, picture numbers 6200 – 6500,
  1 kHz modulation
  Audio 2: normal play, picture numbers 6500 – 6900,
  1 kHz modulation
- The DC voltages have been measured with a Digital Multimeter PM2524, still picture, picture number 5530, unless stated otherwise.

c) *PCB layouts*

Most modules in the set have been equipped with doublesided copper pattern and plated–through holes. For each module a PCB layout is drawn, consisting of a drawing of the component side and of the soldering side (chip side) with corresponding copper pattern.

d) *Parts lists*

For each module an electrical parts list is given, stating the service code numbers of the specific electrical components that have been applied on the module.
The code numbers of the standard components (ICs, transistors, diodes, standard resistors, etc.) have been placed on a collective list in Chapter 5.

e) *Service code numbers of the modules*

In this Service Manual service code numbers for the modules have not been mentioned. Please consult you parts supplier.

3. Repair on modules

To enable repair/adjustment on modules use can be made of extension PCBs or extension cables. A survey can be found sub Service Tools in this chapter.

4. Hidden switches

On Analog I/O module U two switches have been applied, hidden for the user.
The function of these switches is :

SK1 : +11V or RC5 signal at pin 8 of the Euro connector.
Factory adjustment is RC5 at pin 8 (switch pressed out).
SK2 : ENCODED CVBS or NOT ENCODED CVBS signal on CVBS OUT connector BNC3. The factory adjustment is ENCODED (switch pressed out).

Please consult the circuit diagram of Analog I/O module U for more details on these switches.

5. The optical deck

The optical deck in the disc drive is composed of various critical components and at the production department adjusted by complicated alignment equipment.
For the time being repair of the Deck Electronics and of the Laser Detection Unit by a service technician is not allowed.
If a failure analysis reveals that the Deck Electronics or LDU are defective, the entire deck should be submitted for repair to the production centre via the Central Repair Procedure of the Concern Service Centre. Please inquire at your parts supplier's for this procedure.
Repairs on the slide drive assy and the Automatic Tilt Control (ATC) assy are possible. See the List of mechanical parts for the correct code numbers.

6. Coding of items

The coding of component items in the service printing of the PCB's can differ from the coding of the items in the circuit diagrams (exept supply module T). On the PCB's, a letter/number coding has been used (e.g. R1, C1) and in the diagram a 4 number coding (e.g. 3001,2001). The table below shows the conversion between both coding systems.

Circuit diagram 4 number coding	**Service printing on PCB** letter/number coding
2 001	**C 1**
001 → item nbr	1 → item nbr
2 → component nbr:	C → component letter:
1 = Unit, battery	= U
2 = capacitor	= C
3 = resistor	= R
5 = coil, trafo, cristal	= S,L,K
6 = diode	= D
7 = transistor, IC	= T,TS,I,IC

WARNINGS

1. **Laser radiation**

   The Laser Detection Unit (LDU) in the optical deck has been equipped with a semiconductor laser. This laser emits **invisible** light which is focussed on the disc by the objective.
   If the objective would be removed in case of repair, the laser light exits from the objective aperture. **Avoid looking directly into the laser beam, as this might cause permanent injury to the eye**.

2. **Replacement of modules**

   Before replacing a module upon repair, first the mains switch should be switched off. This should be done to prevent damage to the circuits on the modules.

3. **Service position of the set**

   If measurements or repair require that the set is placed on its side (90° position), this may only be done when a 6" test disc is played on the optical deck and the front loader has been removed. If a disc with a larger diameter is used (8" or 12"), the risk that the disc will come loose from the turntable (motor) and cause injury to people in the vicinity will be too great. Also ensure that the disc is always locked on the turntable by the magnetic disc clamping piece (see service tools).

   In the above–mentioned 90° position of the set not all signals will be present according to specification. Adjustments and checks for correct functioning are therefore only allowed in the horizontal position of the set.

4. **The 6" test disc**

   The 6" test disc may only be played when the front loader has been removed. With mounted front loader playback of 8" and 12" discs is possible.

MODIFICATION LEVELS

In the entire set various modification levels have been indicated.

1. **Modification level of the set**

   The modification level of the set can be found at the rear of the cabinet.

   a) *Change code on the type number plate*

   Under the type number a letter and digit code is given which looks as follows :

A H	0 2	6 4 3	1 0 1 2 3 4
production centre	change code	week number	serial number

   The change code is preceded by the production centre.

   b) *Modification level on yellow sticker*

   On a yellow sticker a TM code is marked, indicating the modification level, in this case TM3.

TM					
~~1~~	4	7	10	13	16
~~2~~	5	8	11	14	17
~~3~~	6	9	12	15	18

2. **Modification level of the module**

   In the circuit diagram: top right, under the name of the module (e.g. MOD LEVEL 3).
   On the PCB: in the service printing at the component side
   (e.g. ~~1~~ ~~2~~ ~~3~~ 4 5 6 7 8 9 0).
   The modification level is marked then.

3. **Modification level of the software in the EPROMs**

   On various modules EPROMs have been applied, that have been programmed (see survey below).

module	item number	name	program number
Drive Proc (R)	7204	DRIVE	3104 103 6803.4
Control (S)	7202	CONTROL	3104 103 6804.4
*CPU (W)	7201	SYNC	3104 103 6808.0
*CPU (W)	7224	DESCR.	3104 103 6807.0
*CPU (W)	7247	LV DOS #1	3104 103 6805.2
*CPU (W)	7248	LV DOS #2	3104 103 6806.2

*= only for VP415

   The program number of the software has been applied on a sticker on the EPROM.
   The modification level of the software is the last digit of the program number (behind the dot).

The modification level of the software in the Drive and Control EPROMs can also be retrieved by means of an external computer. To achieve this an F–code command "?=" should be sent to the disc drive (see the directions for use, chapter F–CODE COMMANDS : Revision level request).
The feedback of the disc drive is a 5–digit code of the software revision.

Digit 1 = 0
Digit 2 = major level drive
Digit 3 = minor level drive
Digit 4 = major level control
Digit 5 = minor level control

The modification level of the Drive software will then e.g. be 1.5 (digit 2 . digit 3) and of the Control software e.g. 1.4 (digit 4 . digit 5).
The relation with the modification level in the program number is as follows:

	mod. level progr. number	mod. level software revision
Drive	3104 103 6803.4	1.5
Control	3104 103 6804.4	1.4

Each time a change takes place in the software, the modification level will by raised by one.

A survey of the modification levels of the set, the modules and the software can be found in the Service Information, chapter 8.

ADJUSTMENTS

1. General

For each module an adjustment procedure is given for components that are replaced during repair.
If an entire module is replaced, in principle adjustment should not take place, with the exception of HF PROC module K, VIDEO DO CORR module L and ANALOG I/O module U.

Module K : in case of replacement, adjust R3043 (video ampl.)

Module L : in case of replacement, adjust R3050 (MTF)

Module U : in case of replacement, adjust R3305 (R–Y gain) and R3315 (B–Y gain).

Module B : in case of replacement, adjust R3305 and R3315 on Analog I/O module U.

When module H, K, L or Z is replaced, it is advisable to check the CVBS OUT signal (NOT ENCODED) on BNC3 for correct amplitude and correct VITS signals MBI and MBIV. The CVBS OUT signal is described in adjustment 1 of Ananlog I/O module U.
The VITS signals are described in adjustment 2 of Video D.O. Corr. module L.

For amplitude adjustments see Fig 2.1

The adjustments take place without connection of a computer (video overlay) or external video source, unless stated otherwise.

2. Required

To perform the adjustments the following equipment is required:

- Test disc 6" or 8"
- Dual–beam scope with Delayed Timebase
  If available: – vector scope or
  – dual–beam scope with X–deflection via B–channel (e.g. PM3226P)
- Scope probes with 1:10 attenuator, preferable FET probes or probes with a capacitance < 3pF.
- BNC 75Ω terminator (4822 263 60037).

VIDEO ADJUSTMENTS

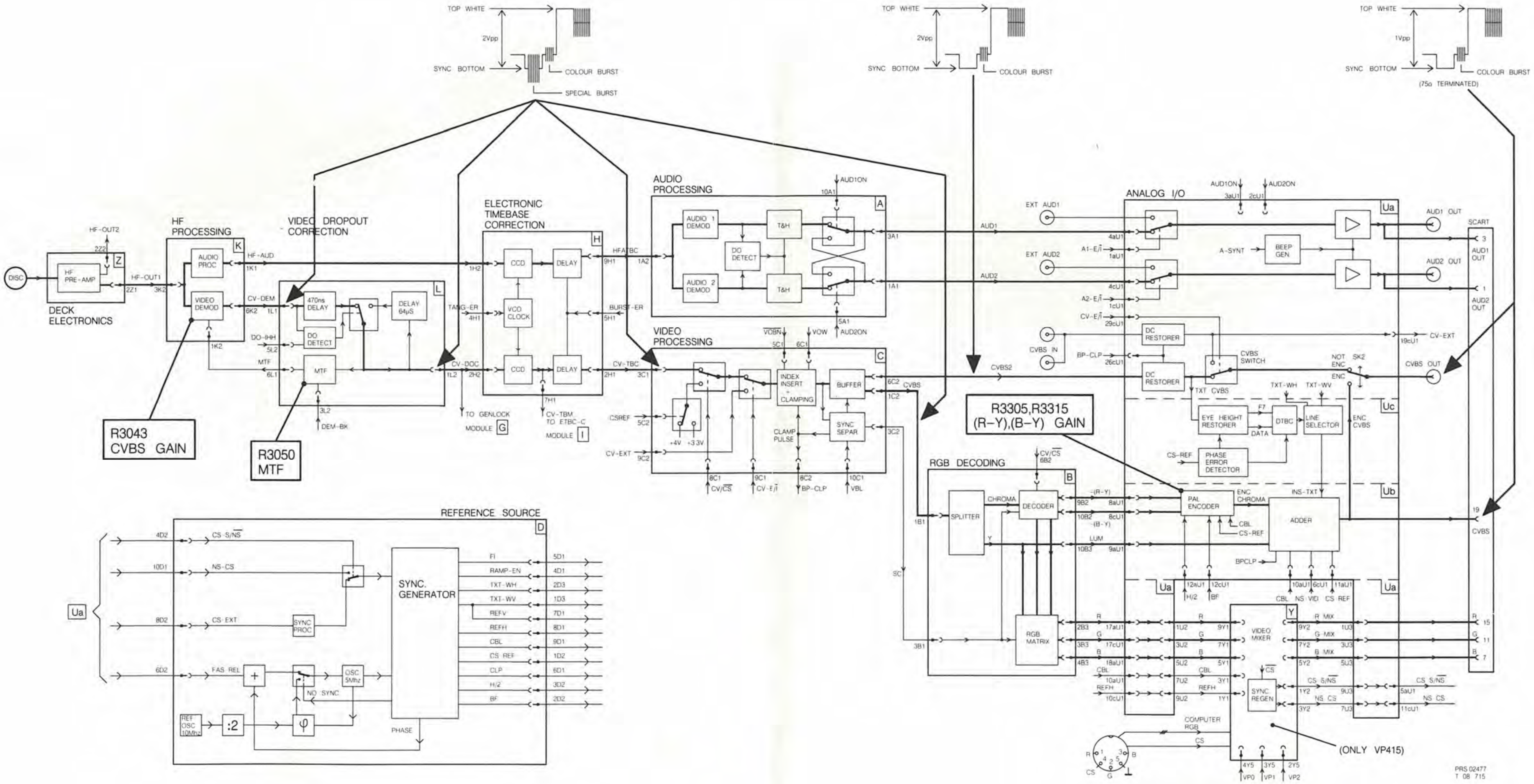
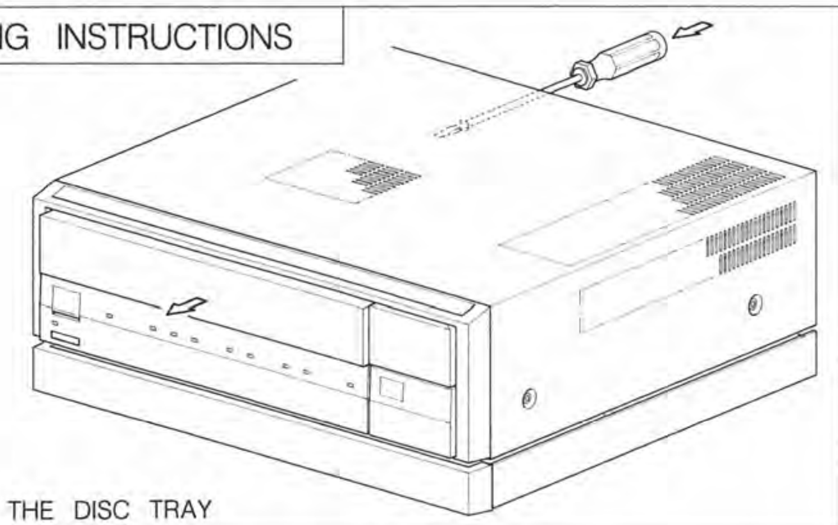
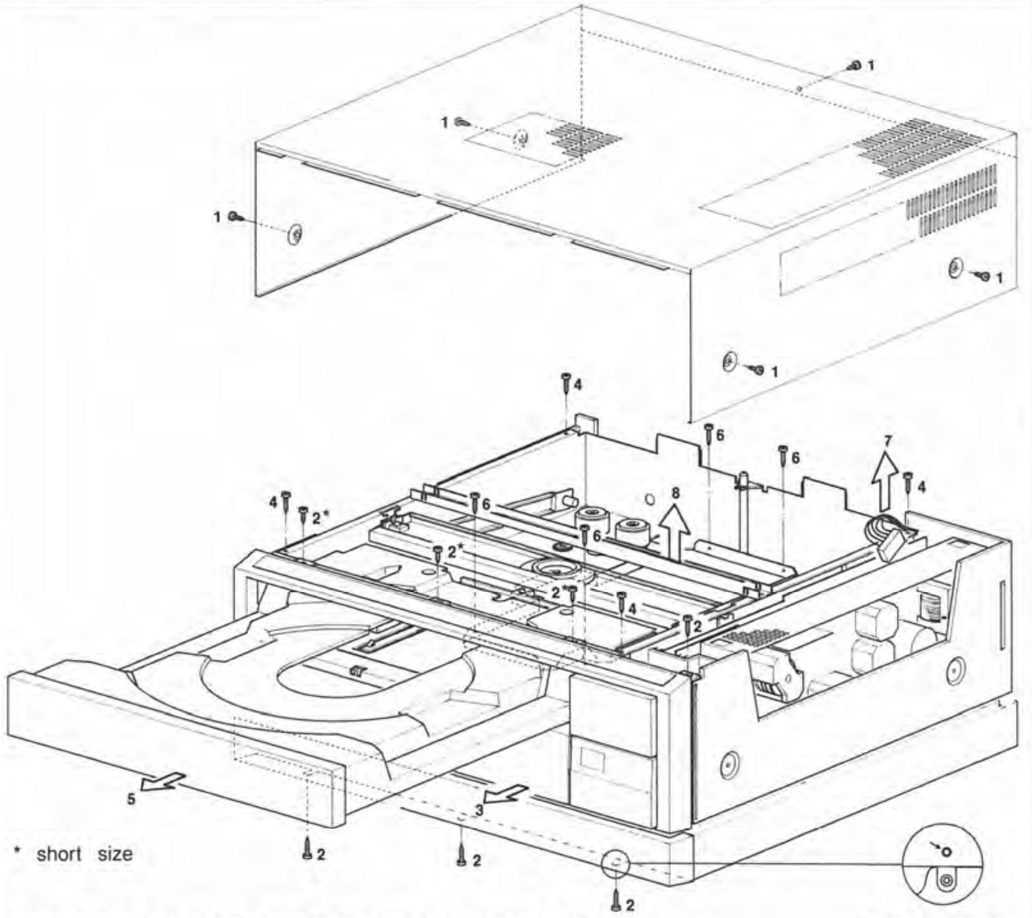


Fig. 21

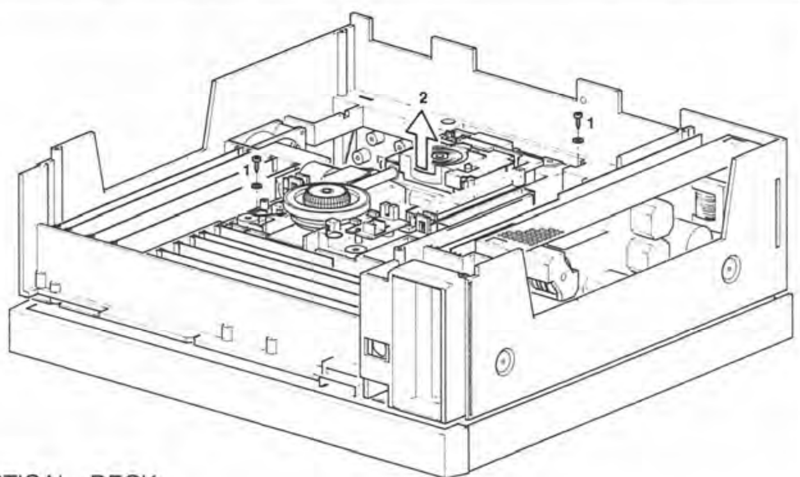
DEMOUNTING INSTRUCTIONS



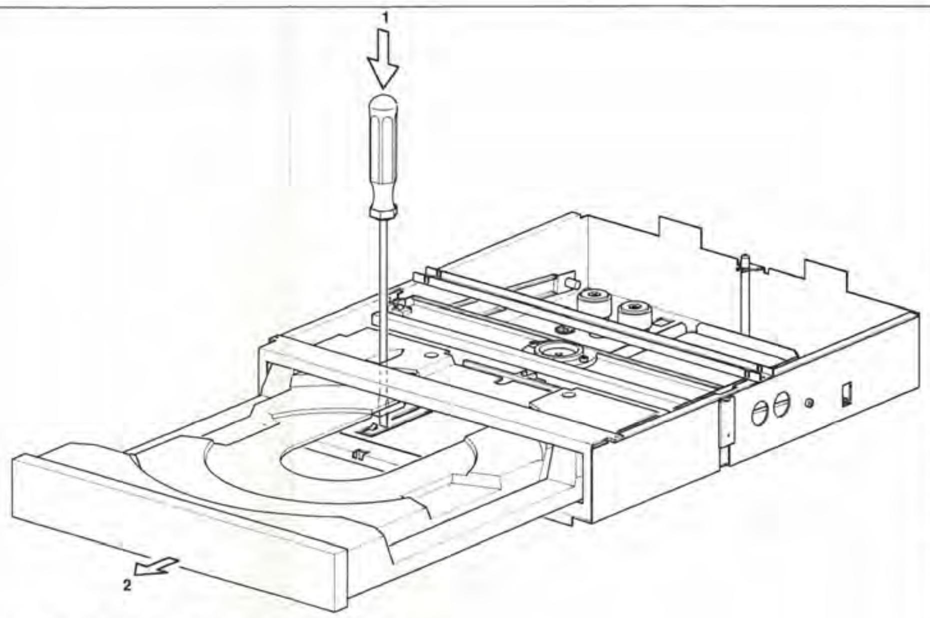
PUSHING OUT THE DISC TRAY



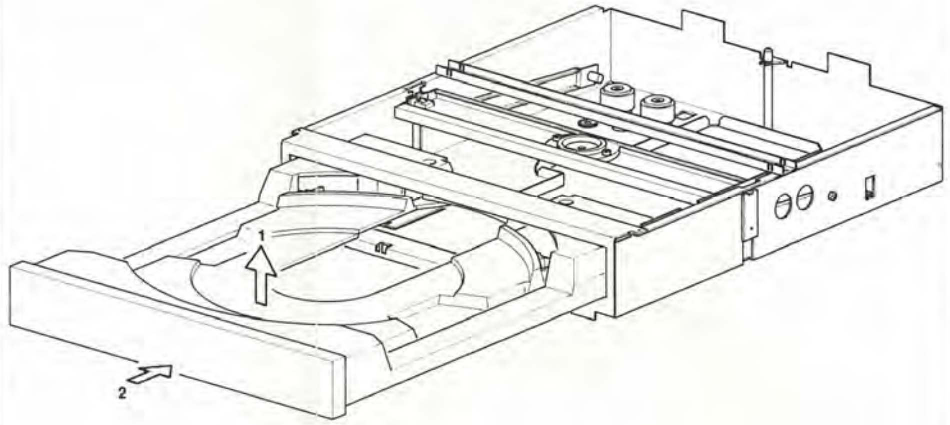
DEMOUNTING UPPERCASETAND FRONTLOADER



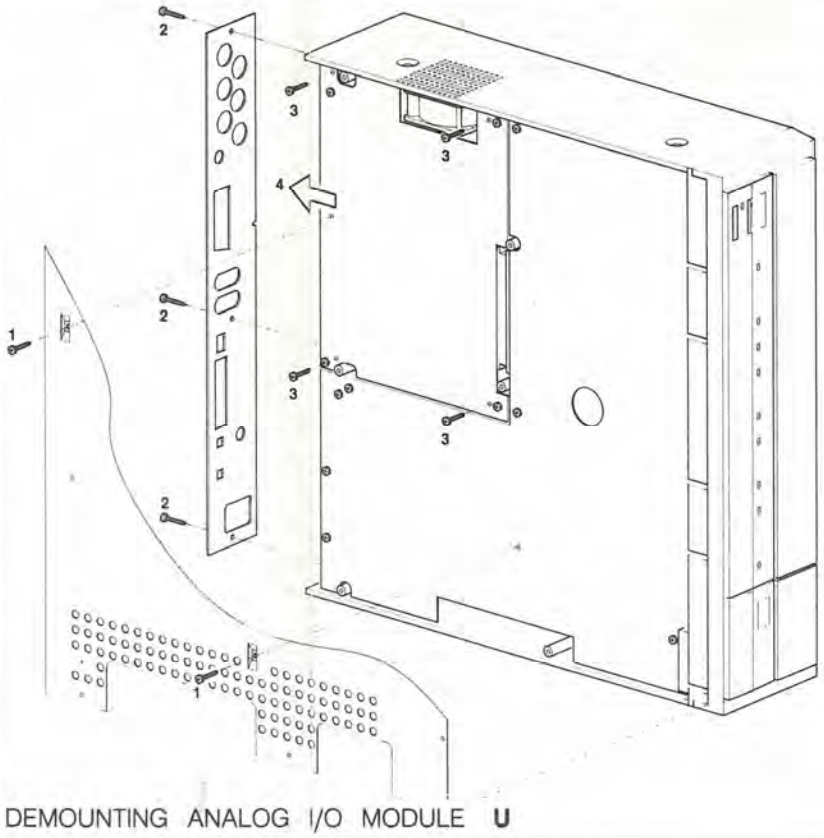
DEMOUNTING OPTICAL DECK



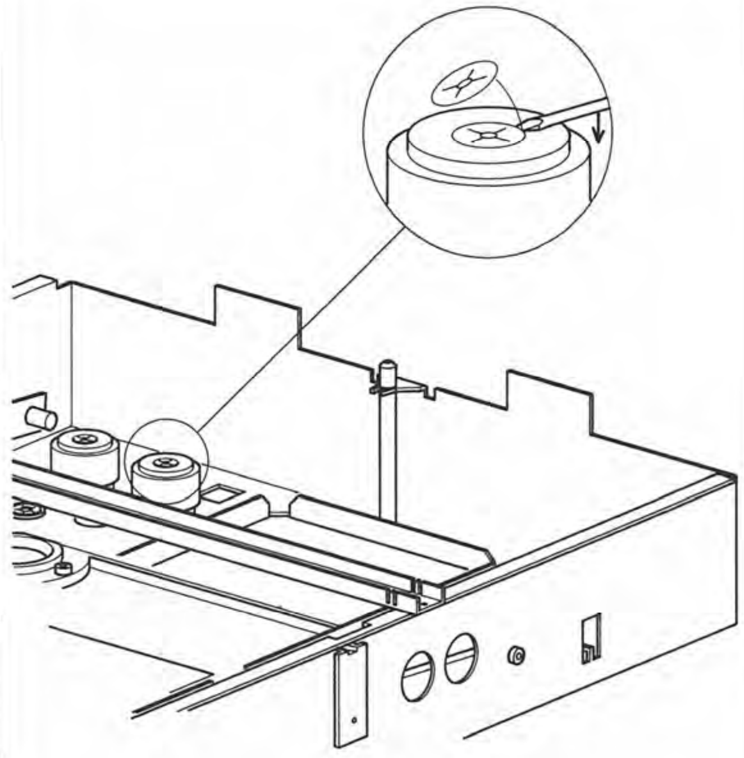
DEMOUNTING DISC TRAY ASSY



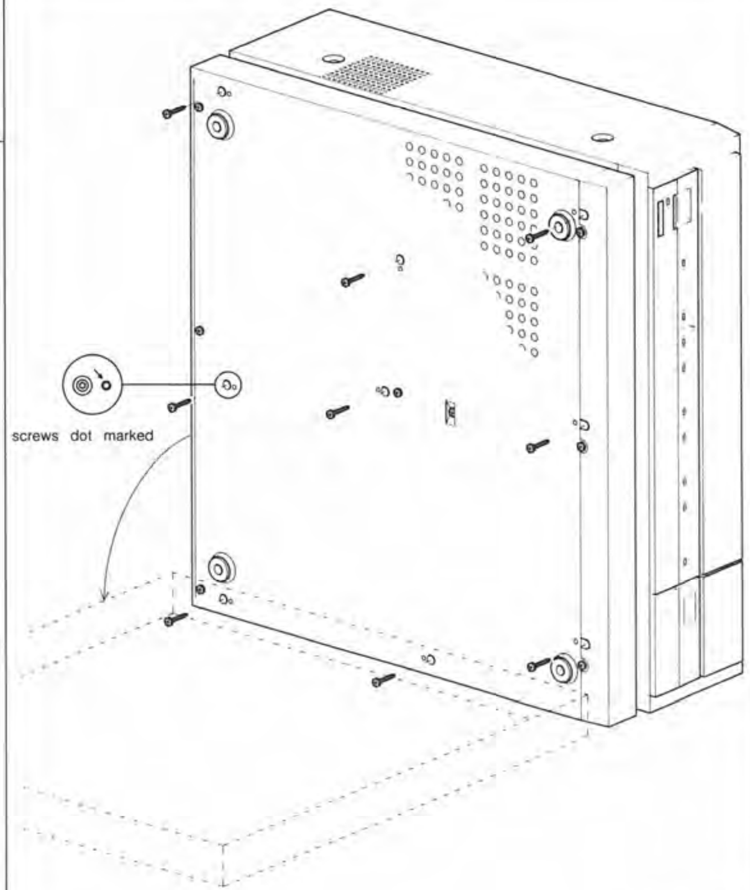
MOUNTING DISC TRAY ASSY



DEMOUNTING ANALOG I/O MODULE **U**



REMOVING SPEEDNUT



ONLY FOR VP415:
DEMOUNTING SANDWICH PART

EVA.00317
T28/710

SERVICE HINTS

WARNING

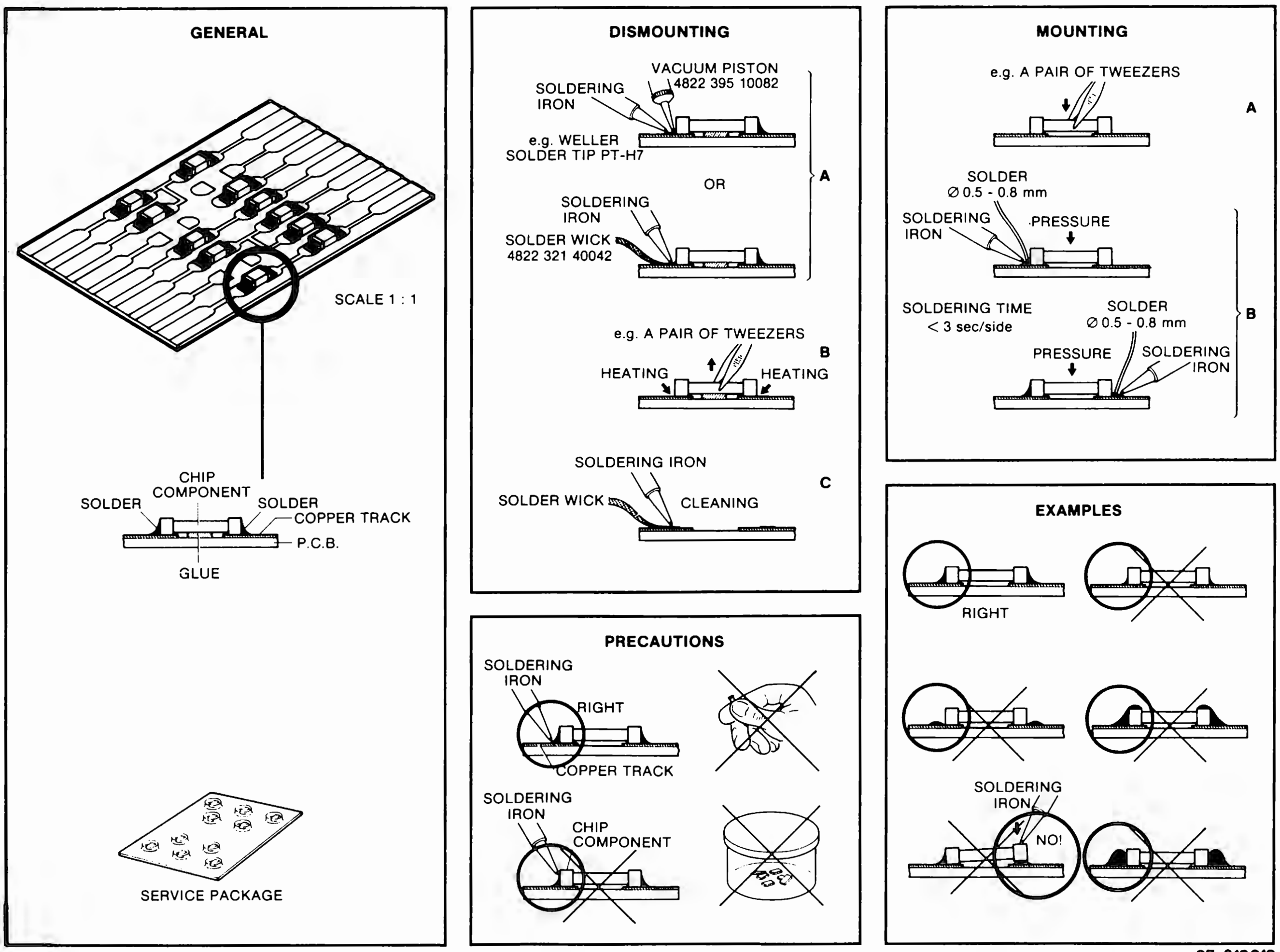
ESD

All ICs and many other semi-conductors are susceptible to electrostatic discharges (ESD).
Careless handling during repair can reduce life drastically.
When repairing, make sure that you are connected with the same potential as the mass of the set via a wrist wrap with resistance.
Keep components and tools also at this potential.

The photodiodes and the laser are more sensitive to electrostatic discharges than MOS IC's.
Careless handling during servicing may reduce life expectacy drastically.
For this reason care should be taken that during servicing the potentials of the tools and yourself are equal to that of the screening of the set

Chip components (SMD)

Chip components have been applied in the set. For the insertion and removal of chip components see the figure below.



27 012C12

TEST DISC 6"
4822 397 30156

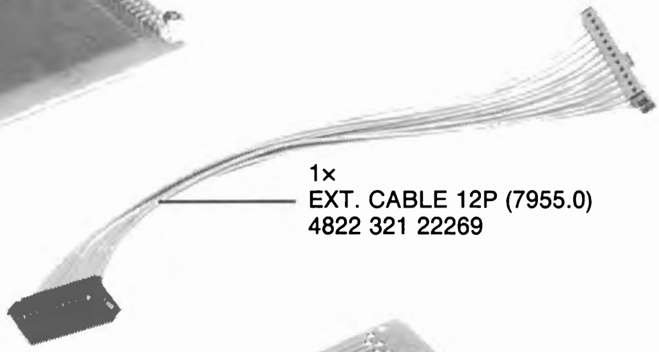
TEST DISC 12" 4822 397 30119
TEST DISC 8" 4822 397 30118

TORX SCREW DRIVER SET
4822 395 50145

REPAIR SET 4822 310 31198

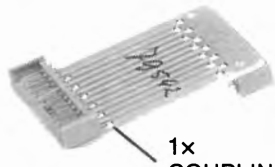
CONTAINING:

2×
EXTENDER PRINT 64P (7949.1)
4822 263 70208

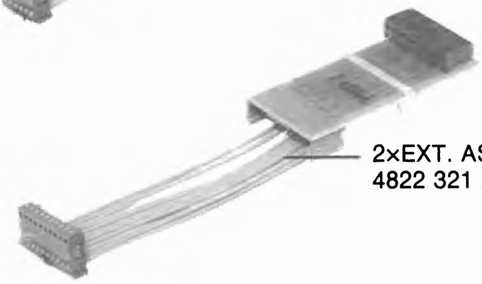


1×
EXT. CABLE 12P (7955.0)
4822 321 22269

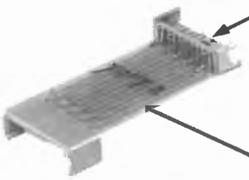
2×
EXT. ASSY 6P (7951.1)
4822 321 22268



1×
COUPLING PIECE 12P (7954.2)
4822 267 50705



2×EXT. ASSY 10P (7950.1)
4822 321 22267



PIN 1,2,3,4
CUT AWAY

1×
COUPLING PIECE
VID MIX (7957.2)
4822 267 50707

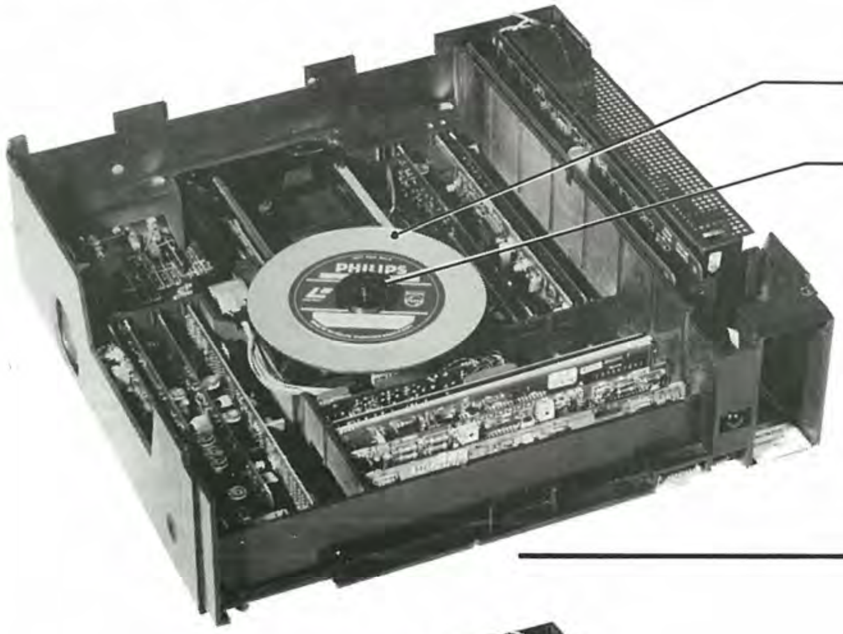
2×
COUPLING PIECE 10P (7953.2)
4822 267 50704

1×
DISC CLAMPING PIECE
4822 532 60775

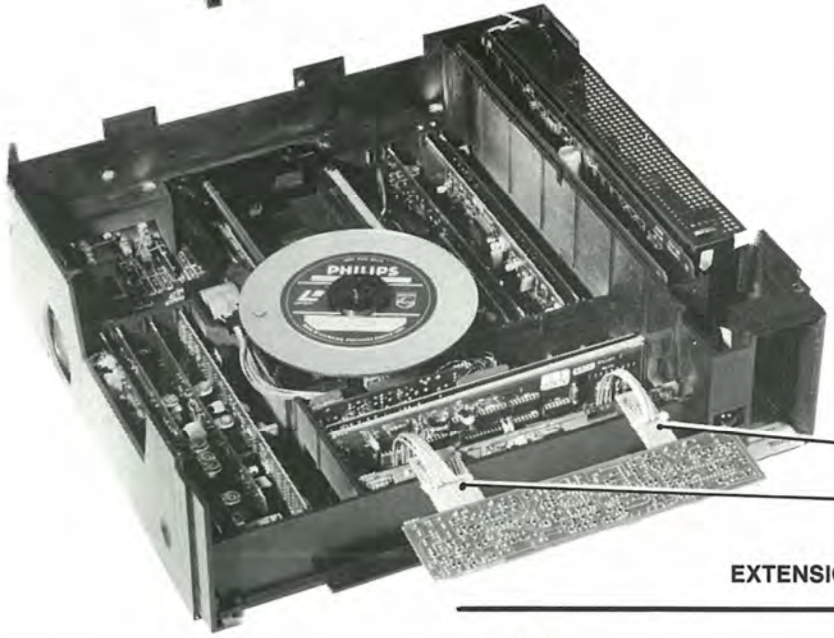
2×
COUPLING PIECE 6P (7952.2)
4822 267 40712

PIN 3 AND 4 INTERCONNECTED
1×
FRONTLOADER SIMULATION
4822 267 50706

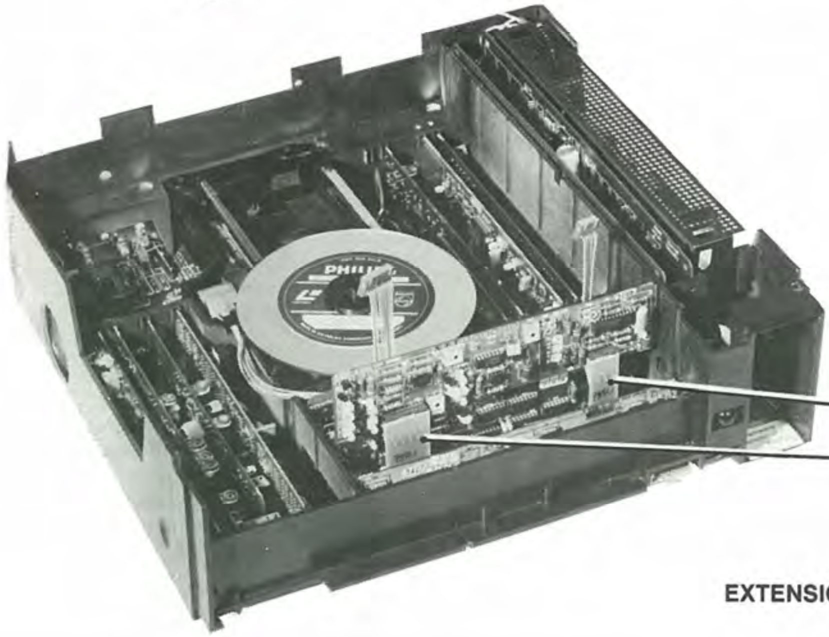
41 832 A



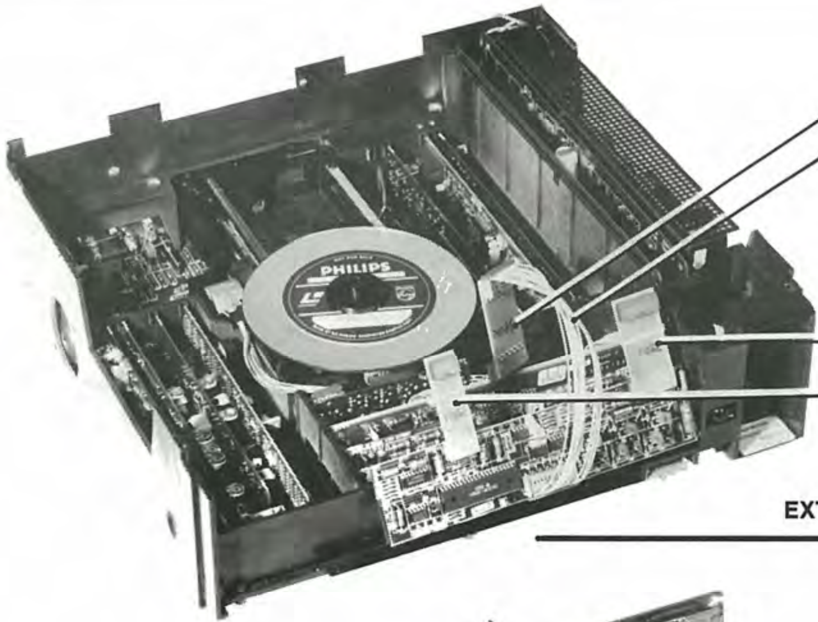
6" TEST DISC



EXTENSION OF MODULE (FLEX)

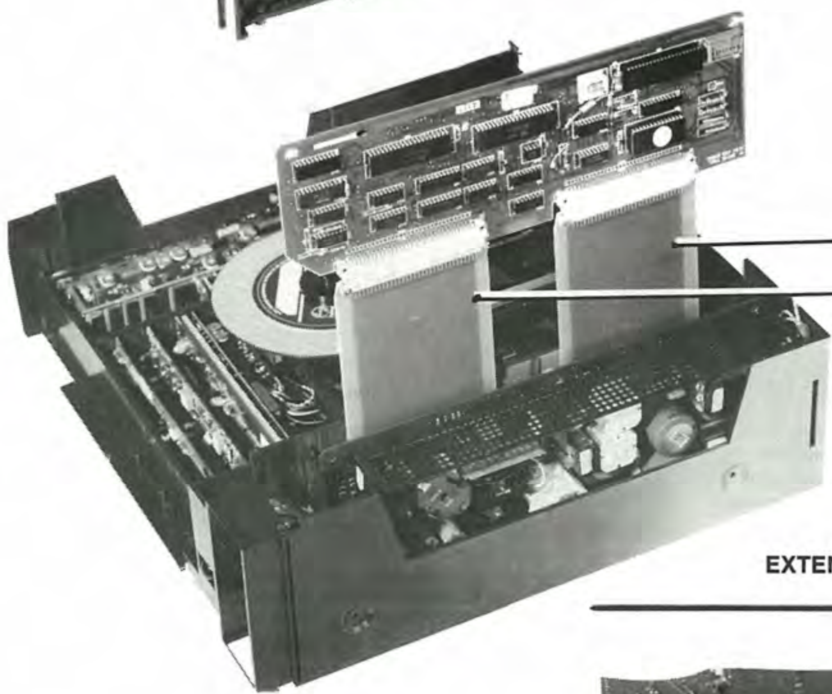


EXTENSION OF MODULE (STEADY)

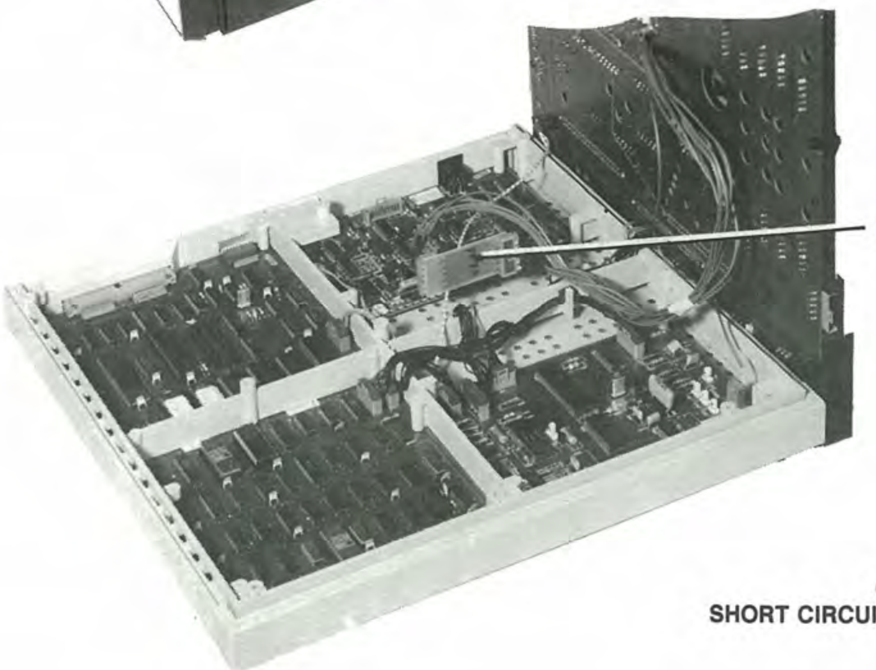


EXTENSION OF MOTOR MODULE

FRONT LOADER
SIMULATION



EXTENSION OF DRIVE/CONTROL MODULE



ONLY VP415
SHORT CIRCUITING OF VID MIX SIGNALS

41 833 B

LIST OF USED SYMBOLS

Safety resistor
Veiligheidsweerstand
Sicherheitswiderstand
Résistance de sécurité

0.2 W ⩽ 220 kΩ - 5%
(CR16) > 270 kΩ - 10%

0.33 W < 1 MΩ - 5%
(SFR25) > 1 MΩ - 10%

0.5 W ⩽ 1 MΩ - 5%
(CR37) > 1 MΩ - 10%

0.33 W - VR25 - 1%

0.5 W ⩽ 1 MΩ - 5%
(CR52) > 1 MΩ - 10%

1 W ⩽ 1.6 MΩ - 5%
(CR68) > 1.6 MΩ - 10%

0.5 W High voltage resistor
(VR37) Hoogspanningsweerstand
Hochspannungswiderstand
Résistance haute tension

Safety capacitor
Veiligheidscondensator
Sicherheitskondensator
Condensateur de sécurité

Ceramic plate capacitor
Keramische plaatcondensator
Keramischer Platten-Kondensator
Condensateur céramique plaquette

Metalized polyester flat film capacitor
Gemetalliseerde polyester condensator
Metallisierter Polyester-Flachkondensator
Condensateur plat à feuille de polyester métallisée

Miniature electrolytic capacitor
Miniatuur electrolytische condensator
Miniatur-Elektrolytkondensator
Condensateur électrolytique miniature

a = 2.5 V	g = 40 V	r = 250 V
b = 4 V	h = 63 V	s = 350 V
c = 6.3 V	j = 100 V	u = 400 V
d = 10 V	l = 125 V	v = 500 V
e = 16 V	m = 150 V	w = 630 V
f = 25 V	q = 200 V	x = 1000 V
		y = 1600 V

Sawtooth pulse converter
Zaagtand-puls omzetter
Sägezahn Impulsumformer
Convertisseur d'impulsions en dents de scie

Pulse-code modulation (6-unit binary code)
Puls code modulatie (6 bits code)
Impulscode-Modulation (6 Bits-code)
Modulation code d'impulsions (code 6 bits)

Puls-duration modulation
Pulslengte modulatie
Impulslänge-Modulation
Modulation de durée d'impulsion

Sync separator
Sync scheider
Sync-Trenner
Séparateur sync

FM detector
FM detector
FM-Detektor
Détecteur FM

Phase discriminator
Fasediscriminator
Phasenvergleich
Discriminateur de phase

Detector
Detector
Detektor
Détecteur

Level detector
Niveau detector
Niveau-Detektor
Détecteur de niveau

Phase-changing network
Faseverschuiver
Phasenverschiebung
Circuit de déphasage

Rejection filter
Bandsperfilter
Bandsperrefilter
Filtre de suppression

Bandpass filter
Band-doorlatend filter
Bandpassfilter
Filtre passe-bande

Low-pass filter
Laag-doorlatend filter
Tiefpassfilter
Filtre passe-bas

Mixer stage
Mengtrap
Mischstufe
Etage mélangeur

High-pass filter
Hoog-doorlatend filter
Hochpassfilter
Filtre passe-haut

HF generator
HF generator
HF-Generator
Générateur HF

Sawtooth generator
Zaagtandgenerator
Sägezahngenerator
Générateur en dents de scie

Square wave generator
Pulsgenerator
Rechteckgenerator
Générateur d'impulsions rectangulaires

Delay element
Vertragingselement
Verzögerungselement
Elément à retard

Limiter
Begrenzer
Begrenzer
Limiteur

Positive-going step function
Positieve flank
Übergang von tief zu hoch
Fonction de palier en sens positif

Negative-going step function
Negatieve flank
Übergang von hoch zu tief
Fonction de palier en sens négatif

Emitter follower
Emitter volger
Emitter folger
Emetteur suiveur

Automatically controlled amplifier
Automatisch gestuurde versterker
Automatisch gesteuerter Verstärker
Amplificateur à commande automatique

Mixer stage
Mengtrap
Mischstufe
Etage mélangeur

Amplifier
Versterker
Verstärker
Ampli

Differential amplifier
Verschilversterker
Differentialverstärker
Ampli différentiel

Amplifier with open output
Versterker met open uitgang
Verstärker mit offenem ausgang
Ampli a sortie ouverte

ELectronic switch
Electronische schakelaar
Elektronische Schalter
Commutateur électronique

Electronic switch
Electronische schakelaar
Elektronischer Schalter
Commutateur électronique

Common control block
Gemeenschappelijk controleblok
Gemeinschaftlicher Kontrolleblock
Bloc de contrôle commun

SRG — Shift register / Schuif register / Schieberegister / Registre à décalage

Q — Output / Uitgang / Ausgang / Sortie

◇ — Open collector output / Open kollektor uitgang / Offenen Kollektor ausgang / Sortie collecteur ouvert

G — Command input / Kommando ingang / Kommando eingang / Entrée ordres

CE — Chip enable input / Chip enable ingang / Chip enable eingang / Entrée chip validation

00 — Bidirectional / Tweezijdig gevoelig / Doppelseitig empfindlich / Bidirectionel

Invertor
Inverter
Inverter
Invertisseur

Or gate
Of-poort
Oder
Porte ou

A	B	x
0	0	0
0	1	1
1	0	1
1	1	1

Nor gate
"Nor"
"Nor"
Porte Non-ou

A	B	x
0	0	1
0	1	0
1	0	0
1	1	0

And gate
En-poort
Und Gatter
Porte Et

A	B	x
0	0	0
0	1	0
1	0	0
1	1	1

Nand gate
"Nand"
"Nand"
Porte "Non-Et"

A	B	x
0	0	1
0	1	1
1	0	1
1	1	0

Buffer
Buffer
Puffer
Tampon

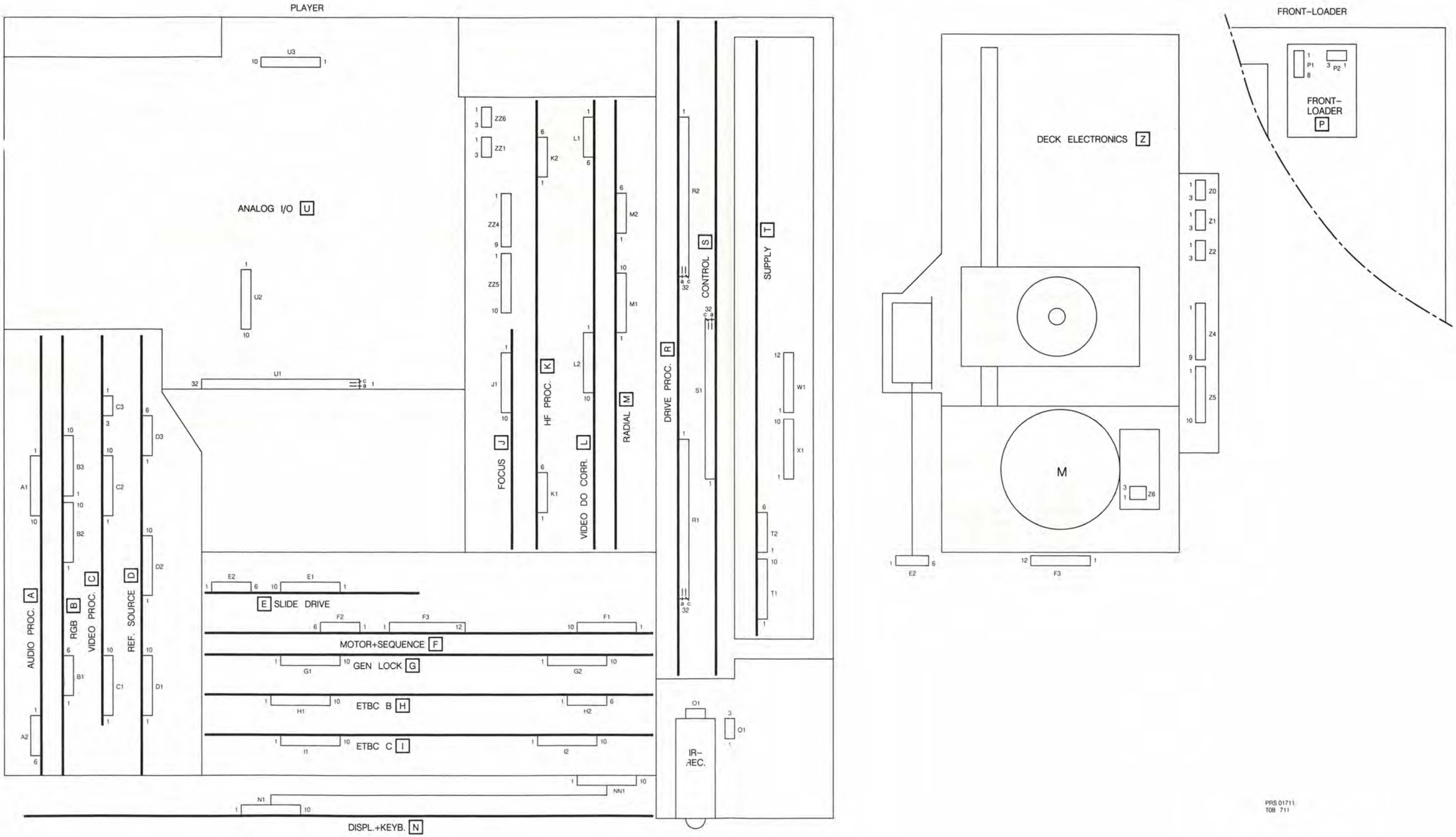
Inverting buffer
Inverterende buffer
Invertierender puffer
Tampon invertisseur

Buffer with open output
Buffer met open uitgang
Puffer mit offenem ausgang
Tampon à sortie ouverte

Module– and connector lay–out
Signal listing
Wiring diagram
Blockdiagram Control routes
Blockdiagram AUDIO/VIDEO signal path
Blockdiagram Servo

Chapter 3

MODULE AND CONNECTOR LAY OUT



ALPHABETICAL SIGNAL LISTING

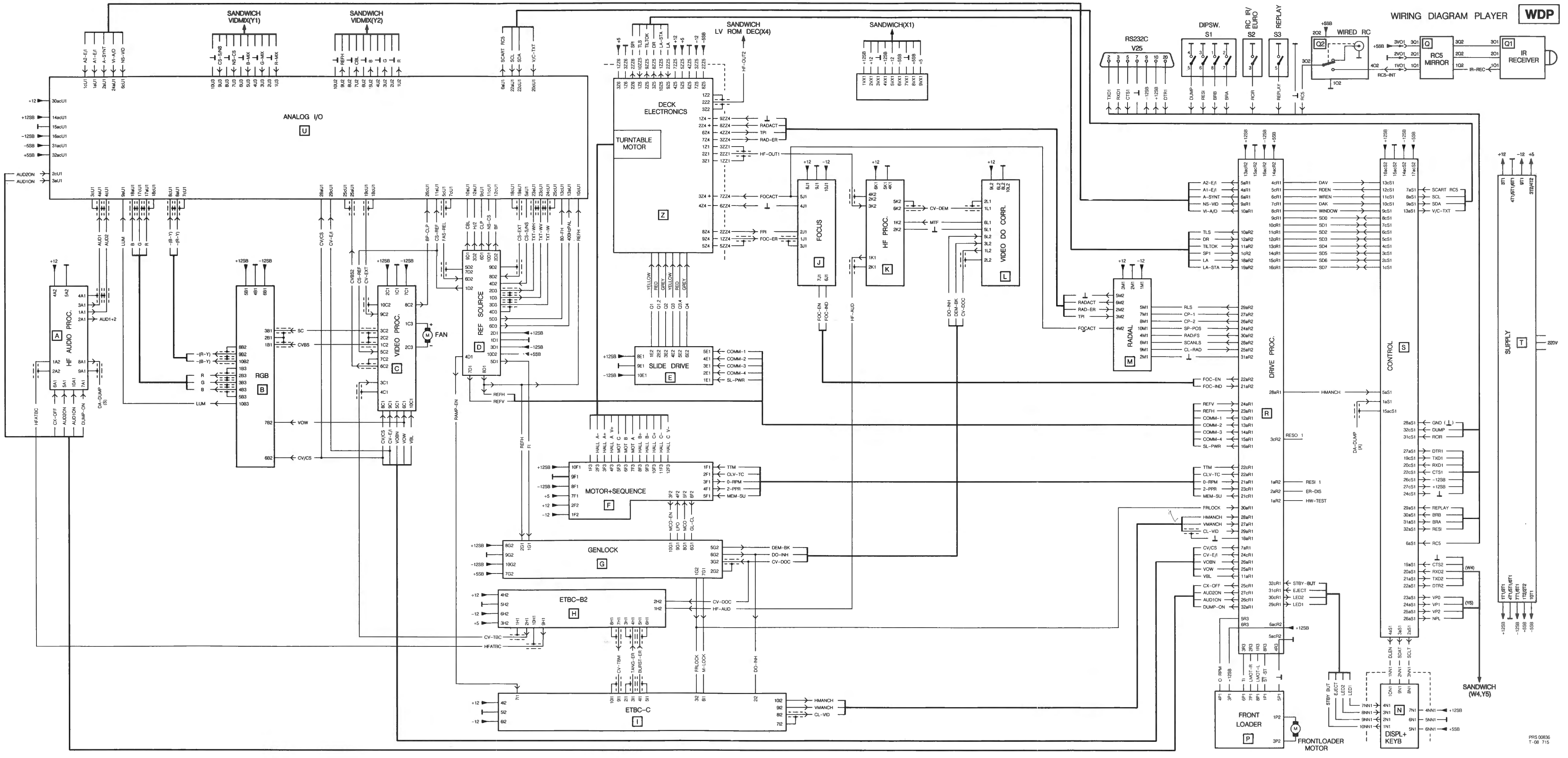
-(B-Y)	Colour difference B-Y	
-(R-Y)	Colour difference R-Y	
+12	Switched +12V	
+12SB	+12V standby supply	
+5	Switched +5V	
+5SB	+5V standby supply	
0-RPM	0 RPM status	0V = 0 RPM
-12	Switched -12V	
-12SB	-12V standby supply	
2-PPR	2 pulses per revolution	pos.pulses
400Hz PAL	PAL switching signal	
-5SB	-5V standby supply	
80-FH	80 times horizontal freq.	
A1-E/I	Audio 1 internal/external	+12V = ext
A2-E/I	Audio 2 internal/external	+12V = ext
ALE	Address latch enable	
A-SYNT	Synthesised audio on/off	+12V = on
ATN	Attention	0V = active
AUD1	Audio 1	
AUD1+2	Audio 1 + audio 2	
AUD1ON	Audio 1 on/off	+12V = on
AUD2	Audio 2	
AUD2ON	Audio 2 on/off	+12V = on
B	Blue video signal	
BF	Burst flag	pos.pulses
B-MIX	Blue video signal from mixer	
BP-CLP	Bypass clamp	pos.pulses
BRA	Baudrate select A	0V / +5V
BRB	Baudrate select B	0V / +5V
B-TTL	Blue video signal TTL level	
BURST-ER	Burst error signal	
CBL	Composite blanking	pos.pulses
CLCF	Bit clock CIM to FIL	
CLDE	Bit clock DEMOD to ERCO	
CLEC	Bit clock ERCO to CIM	
CLOX	LV-ROM decoder master clock	
CLP	Clamp pulse	pos.pulses
CL-RAD	Clipped radial	-12V / +12V
CL-VID	Clipped video	0V / +12V
CLV-TC	CLV trackcross	+5V = active
COMM1	Commutation coil 1	+5V = on
COMM2	Commutation coil 2	+5V = on
COMM3	Commutation coil 3	+5V = on
COMM4	Commutation coil 4	+5V = on
CP-1	Course pulse 1	0V = active
CP-2	Course pulse 2	0V = active
CS	Composite sync	
CS 1-8	Chip select 1 up to 8	
CS-EXT	External comp. sync input	
CS-REF	Composite sync reference	pos.pulses
CS-S/NS	Standard/non standard CS select	+5V = standard
CS-TTL	Comp. sync TTL level	
CTS	Clear to send (RS232)	
CTS1	CTS	
CTS2	CTS	
CTS3	CTS	
CV/CS	CVBS/Comp. Sync select	+12V = CVBS
CVBS IN	External CVBS input signal	
CVBS	Composite video/burst/sync	
CVBS OUT	CVBS output signal	
CVBS2	Disc CVBS without special burst	
CVBS-INT	Internal CVBS	
CV-DEM	CVBS demodulated	
CV-DOC	CVBS dropout corrected	
CV-E/I	CVBS external/internal select	+12V = external
CV-EXT	External CVBS	
CV-TBC	CVBS time base corrected	
CV-TBM	CVBS time base measurement	
CX-OFF	CX on/off	+12V = off
DADE	Data DEMOD to ERCO	
DA-DUMP	Data disc dump	
DAEC	Data ERCO to CIM	
DAK	S-bus data acknowledge	
DAV	S-bus data available	
DB/STAT	Databit/status text insert	0V = busy
DEM-BK	Demodulator burst key	pos.pulses
DEMV	Demodulated vert. pulse	

DLCF	Data left CIM to FIL	
DLEN	P-bus data line enable	+5V = active
DO-INH	Dropout protection inhibit	+12V = active
DR	Disc reflection	+5V = refl
DRCF	Data right CIM to FIL	
DTR	Data terminal ready (RS232)	
DTR 3	DTR	
DTR 1	DTR	
DTR 2	DTR	
DUMP	Dump on/off switch	0V = dump on
DUMP-ON	Data dump on/off	+12V = on
EJECT	Eject button	0V = active
ELCF	Error flag left	
ERCF	Error flag right	
ER-DIS	Error display	0V = active
EXT AUD 1	External audio 1	
EXT AUD 2	External audio 2	
FAS-REL	Phase relation	
FI	Field identification	
FOCACT	Focus actuator drive signal	
FOC-EN	Focus enable	+12V = enable
FOC-ER	Focus error	
FOC-IND	In focus indication	0V = in focus
FPI	Focus position indication	-12V = in position
FRLOCK	Frame lock	+5V = in lock
FSDE	Frame sync DEMOD to ERCO	
FSEC	Frame sync ERCO to CIM	
G	Green video signal	
GLC	Genlock clock (4.5MHz)	
GL-CL	Genlock clock (4.5MHz)	
G-MIX	Green video signal from mixer	
G-TTL	Green video signal TTL level	
H/2	PAL 8kHz pulse	
HALL C-	»	
HALL B-	»	
HALL C+	»	
HALL B+	»	
HALL AV+	» signals from HALL elements	
HALL A-	»	
HALL A+	»	
HALL CV-	»	
HFATBC	HF audio timebase corrected	
HF-AUD	HF audio	
HF-OUT 1	HF signal disc drive	
HF-OUT 2	HF signal sandwich	
HMANCH	Horizontal sync	neg.pulses
HOR. BL.	Horizontal blanking adjustment	
HW-TEST	Hardware test	
INS-TXT	TXT signal for insert	
IRQ	Interrupt request	
IR-REC	RC5 from IR receiver	
LA	Laser on/off	0V = off
LA-STA	Laser status	0V = on
LDI	Load index	
LED1	LED drive	
LED2	LED drive	
LMOT-L	Load motor left	+5V = on
LMOT-R	Load motor right	+5V = on
LPO	Line pulse out	
LPWM	Line pulse width modulated	
LUM	Luminance	
MCES	Motor control error signal	
MCO	Motor control output	
MCO-EN	MCO enable	+12V = active
MEM-SU	Memory start up	+5V = active
M-LOCK	Motor lock	
MOT C	»	
MOT B	» Motor drive signals	
MOT A	»	
MTF	Motional transfer function	
NPL	Normal play forward	+5V = active
NS-CS	Non standard composite sync	
NS-VID	Non standard video indication	+12V = NSV
OBF	Output buffer full	
OBS	Output burst switch NTSC	+12V = active
PWM	Pulse width modulated	
Q1	Stepping motor coil 1 (Yellow)	
Q1,2	Common 1,2 (Red)	
Q2	Stepping motor coil 2 (Grey)	

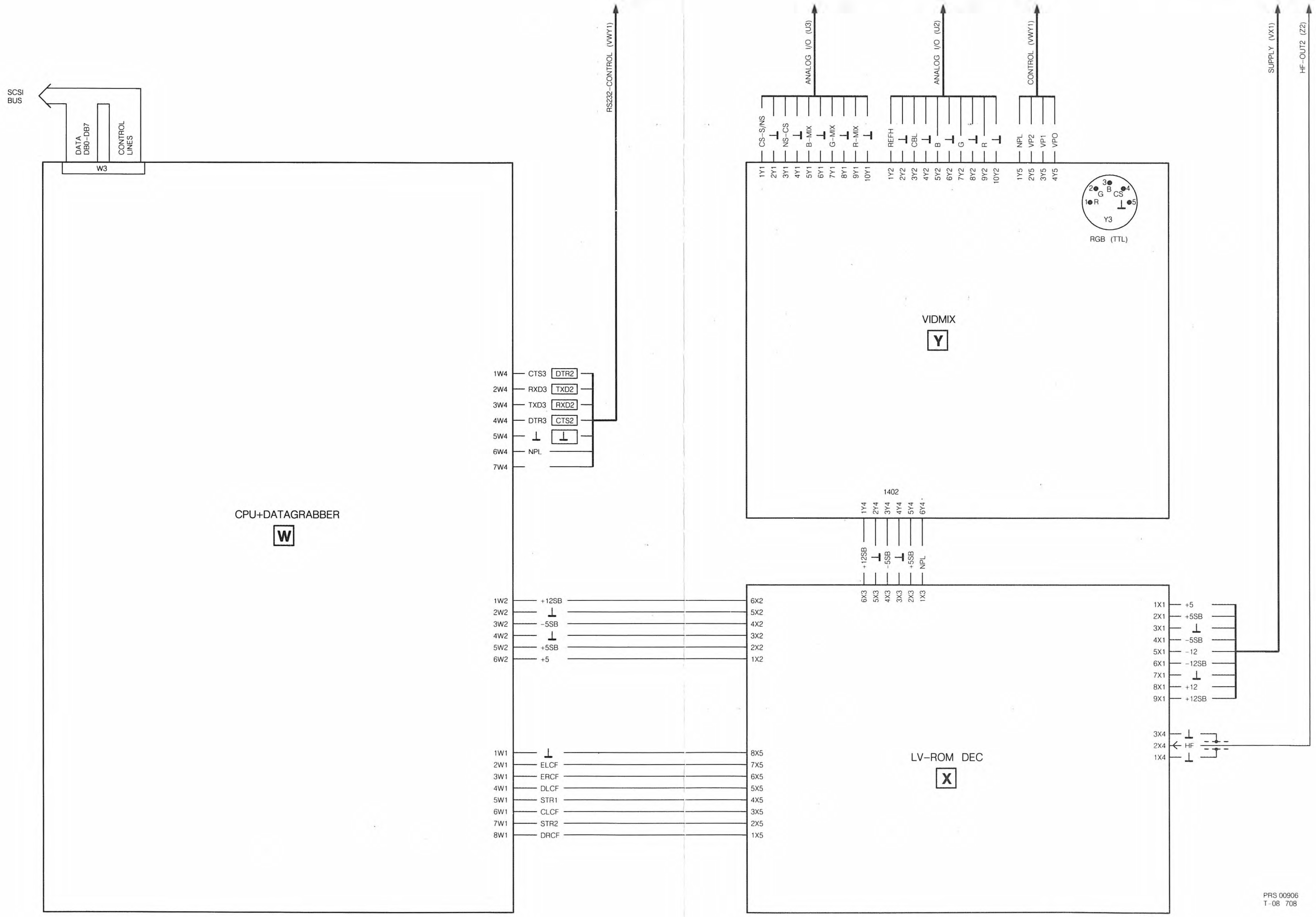
Q3	Stepping motor coil 3 (Yellow)	
Q3,4	Common 3,4 (Red)	
Q4	Stepping motor coil 4 (Grey)	
R	Red video signal	
RADACT	Radial actuator drive signal	
RAD-ER	Radial error	
RAD-FS	Radial filter select	0V = low pass
RAMP-EN	Ramp enable	pos.pulses
RC5 IN(B)	RC5 input SCART	
RC5	RC5 commands	
RC5-INT	RC5 from IR receiver	
RC5-SCART	RC5 commands SCART	
RC5-OUT	RC5 output control	
RCIR	RC input IR/SCART	+5V = IR
RD	Read	
RDEN	S-bus read enable	
RD-STRT	Read start pulse text insert	+5V = inactive
REF-CLP	Clamp	
REFH	Horizontal reference	pos.pulses
REFV	Vertical reference	pos.pulses
REPLAY	Replay switch on/off	0V = replay
RESI	Reserved input dipswitch	
RESI 1	Reserved input drive	
RESO 1	Reserved output drive	
RESUPI	Reset UPI	
RGB-STA	RGB status signal SCART	
RLS	Radial loop switch	+0V = closed
R-MIX	Red video signal from mixer	
R-TTL	Red video signal TTL level	
RXD	Recieved data (RS232)	
RXD1	RXD	
RXD2	RXD	
RXD3	RXD	
SC	Sandcastle pulse	pos.pulses
SCANLS	Scan loop switch	0V = active
SCL	IIC bus clock	
SCLT	P-bus clock	
SCSI	Small computer system interface	
SD 0-7	S-bus data	
SDA	IIC bus data	
SDAT	P-bus data	
SEL	Selection	
SL-PWR	Slide power low/high	+5V = low
SMF	Switch mode frequency	17,6 kHz

SPI	Slide position indication	0V = inwards
SP-POS	Spot position	
SSDE	Symbol sync DEMOD to ERCO	
ST-ST	Start-stop switch	0V = start
STB	Strobe	0V = active
STBY	Standby command	0V = standby
STBY-BUT	Standby button command	
STR1	Strobe 1 (16 bit word)	
STR2	Strobe 2 (8 bit word)	
SYNC IN	External sync input signal	
SYNC OUT	Sync output signal	
TANG-ER	Tangential error	
TI	Tray inside	0V = inside
TILTOK	Tilt in position	0V = in position
TLS	Tilt loop switch	+5V = closed
TPI	Track position indication(+6/-6V)	-6V = on track
TSP	Terminal speed	
TTM	Turntable motor on/off	+5V = on
TX/RX	Transmit/receive data	0V = receive
TXD	Transmit data (RS232)	
TXD1	TXD	
TXD2	TXD	
TXD3	TXD	
TXT-IW	Teletext insertion window	
TXT-WH	Teletext window horizontal	pos.pulses
TXT-WV	Teletext window vertical	pos.pulses
UNEC	Unreliable data ERCO to CIM (Error flag)	
V/C-TXT	Video/control text insert	+5V = video text
VBL	Vertical blanking	neg.pulses
VI-A/D	Video analogue/digital	+12V = analogue
VI-DOP	Video dropout pulse	
VMANCH	Vertical sync	neg.pulses
VOBN	Video background insertion	0V = active
VOW	Video character insertion	+5V= active
VP0	Video mixer control 0	
VP1	Video mixer control 1	
VP2	Video mixer control 2	
VR	Vertical reference	
WDOGRS	Watchdog reset	+5V = reset
WINDOW	S-bus window	
WR	Write	
WR-CLK	Write clock text insert	+5V = inactive
WREN	S-bus write enable	

WIRING DIAGRAM PLAYER **WDP**

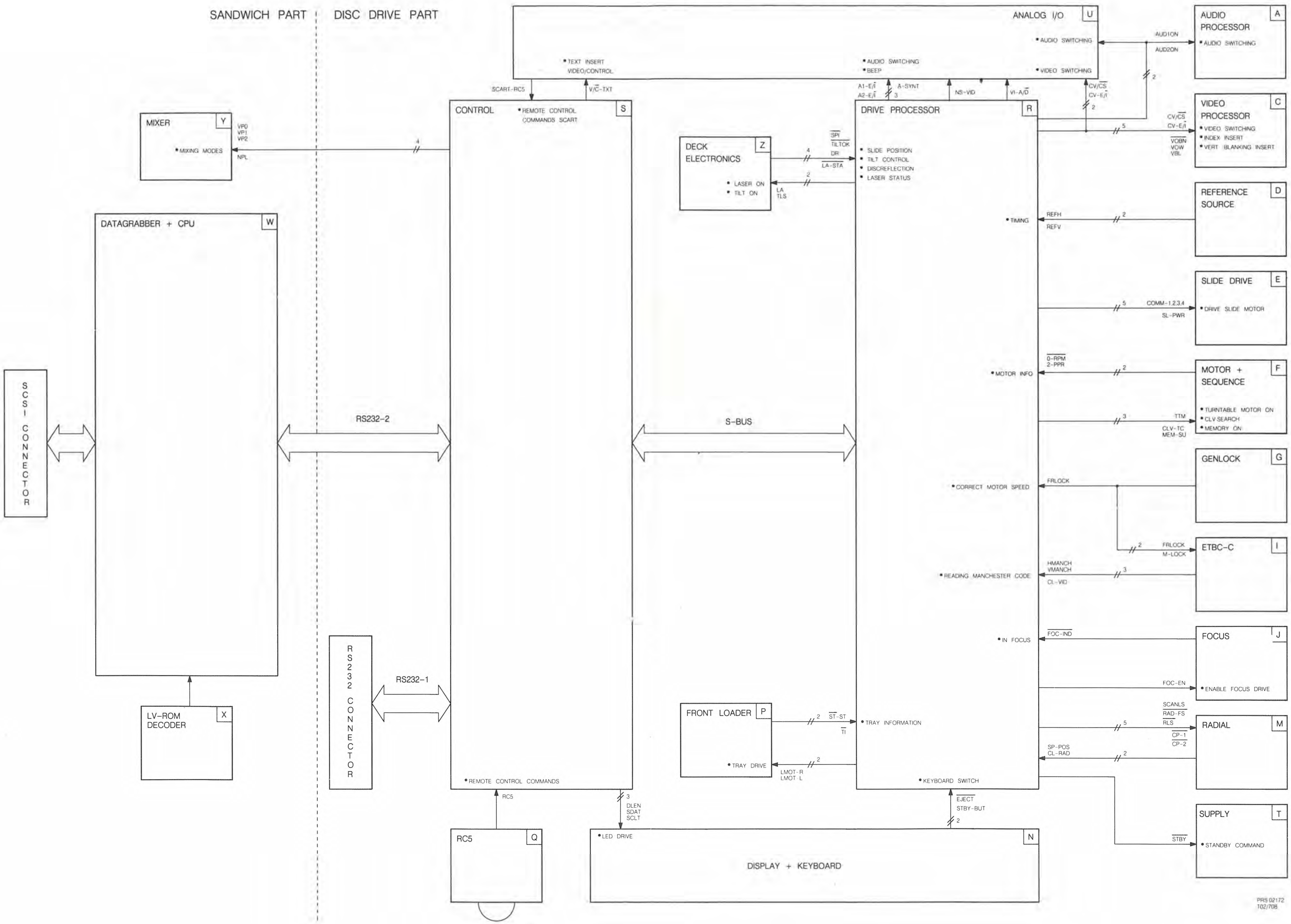


CS 7 831



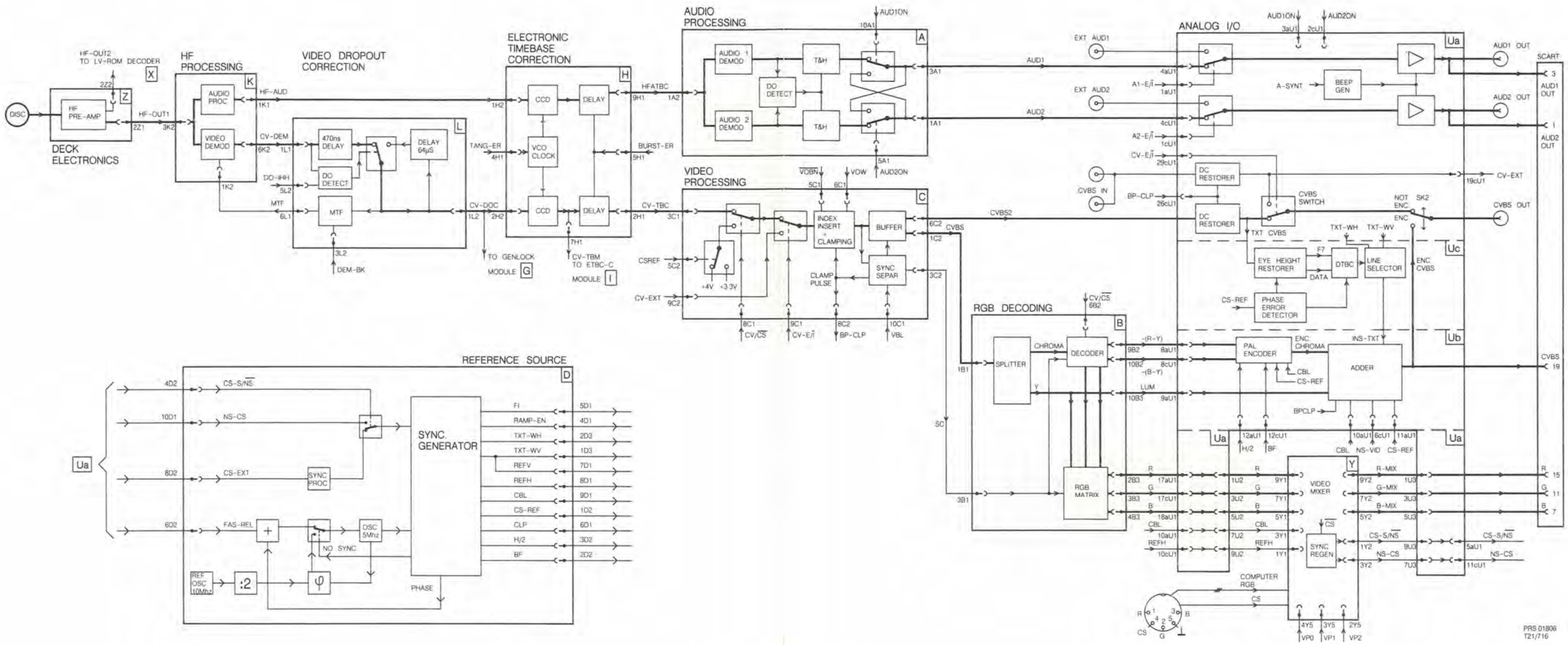
SCSI BUS
DATA DB0-DB7
CONTROL LINES
W3
RS232-CONTROL (VWY1)
CPU+DATAGRABBER
W
1W4 CTS3 DTR2
2W4 RXD3 TXD2
3W4 TXD3 RXD2
4W4 DTR3 CTS2
5W4
6W4 NPL
7W4
1W2 +12SB
2W2
3W2 -5SB
4W2
5W2 +5SB
6W2 +5
1W1
2W1 ELCF
3W1 ERCF
4W1 DLCF
5W1 STR1
6W1 CLCF
7W1 STR2
8W1 DRCF
ANALOG I/O (U3)
ANALOG I/O (U2)
CONTROL (VWY1)
SUPPLY (VX1)
HF-OUT2 (Z2)
CS-S/NS
NS-CS
B-MIX
G-MIX
R-MIX
REFH
CBL
B
G
R
NPL
VP2
VP1
VPO
1Y1 2Y1 3Y1 4Y1 5Y1 6Y1 7Y1 8Y1 9Y1 10Y1
1Y2 2Y2 3Y2 4Y2 5Y2 6Y2 7Y2 8Y2 9Y2 10Y2
1Y5 2Y5 3Y5 4Y5
Y3
RGB (TTL)
VIDMIX
Y
1402
1Y4 2Y4 3Y4 4Y4 5Y4 6Y4
+12SB
-5SB
+5SB
NPL
6X3 5X3 4X3 3X3 2X3 1X3
6X2 5X2 4X2 3X2 2X2 1X2
8X5 7X5 6X5 5X5 4X5 3X5 2X5 1X5
1X1 +5
2X1 +5SB
3X1
4X1 -5SB
5X1 -12
6X1 -12SB
7X1
8X1 +12
9X1 +12SB
3X4
2X4 HF
1X4
LV-ROM DEC
X
PRS 00906
T-08 708

BLOCKDIAGRAM CONTROL ROUTES

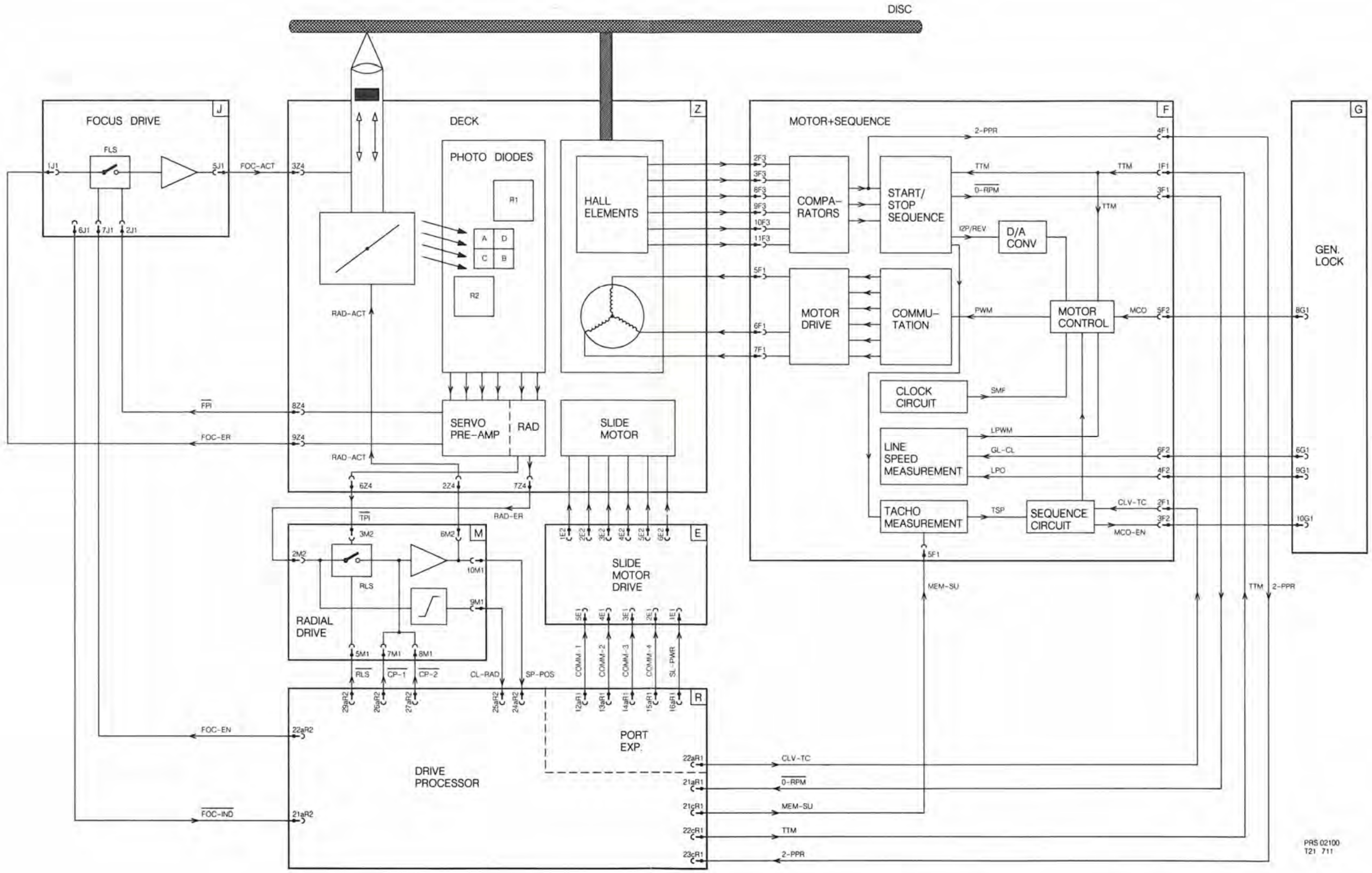


CS 7 833

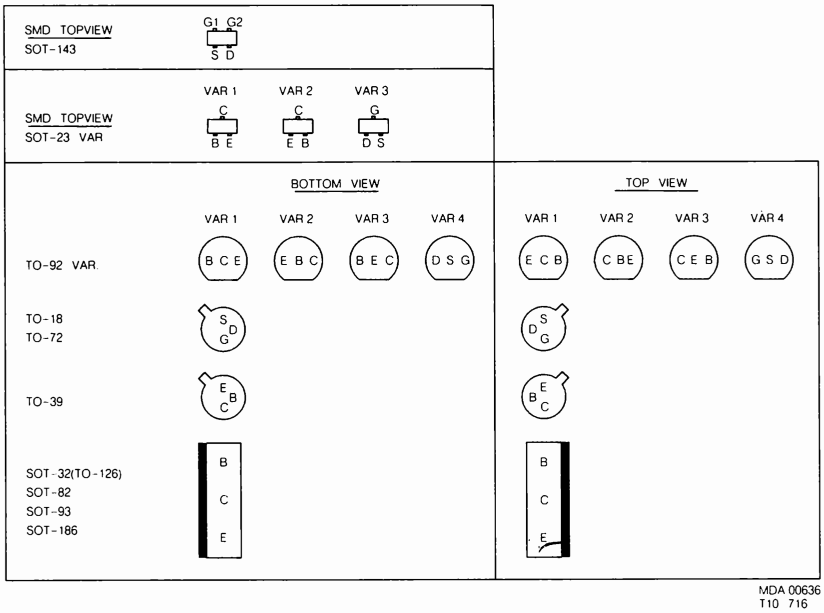
BLOCKDIAGRAM AUDIO/VIDEO PATH



BLOCKDIAGRAM SERVO



CONNECTIONS OF SEMICONDUCTORS



SOT-143	BF992
SOT-186	BUT11F
SOT-23 VAR.1	BC807
	BC817
	BC847
	BC848
	BC849
	BC858
	BC859
	BFS19
SOT-23 VAR.3	BFR30
SOT-32 (TO-126)	BD135
	BD434
	BD435
	BD436
	BD437
	BD438
	BUX86
SOT-82	BUW85
SOT-93	BUW12
TO-18	BSV78
	BSV80
TO-39	BSW68
TO-72	BSD213
TO-92 VAR.1	BC368
	BC369
	BC639
	BC640
TO-92 VAR.2	BC327
	BC337
	BC375
	BC376
	BC546
	BC547
	BC548
	BC549
	BC556
	BC557
	BC558
	BFR54
	PH2369
TO-92 VAR.3	BF450
	BF494
TO-92 VAR.4	BC264
	BF256

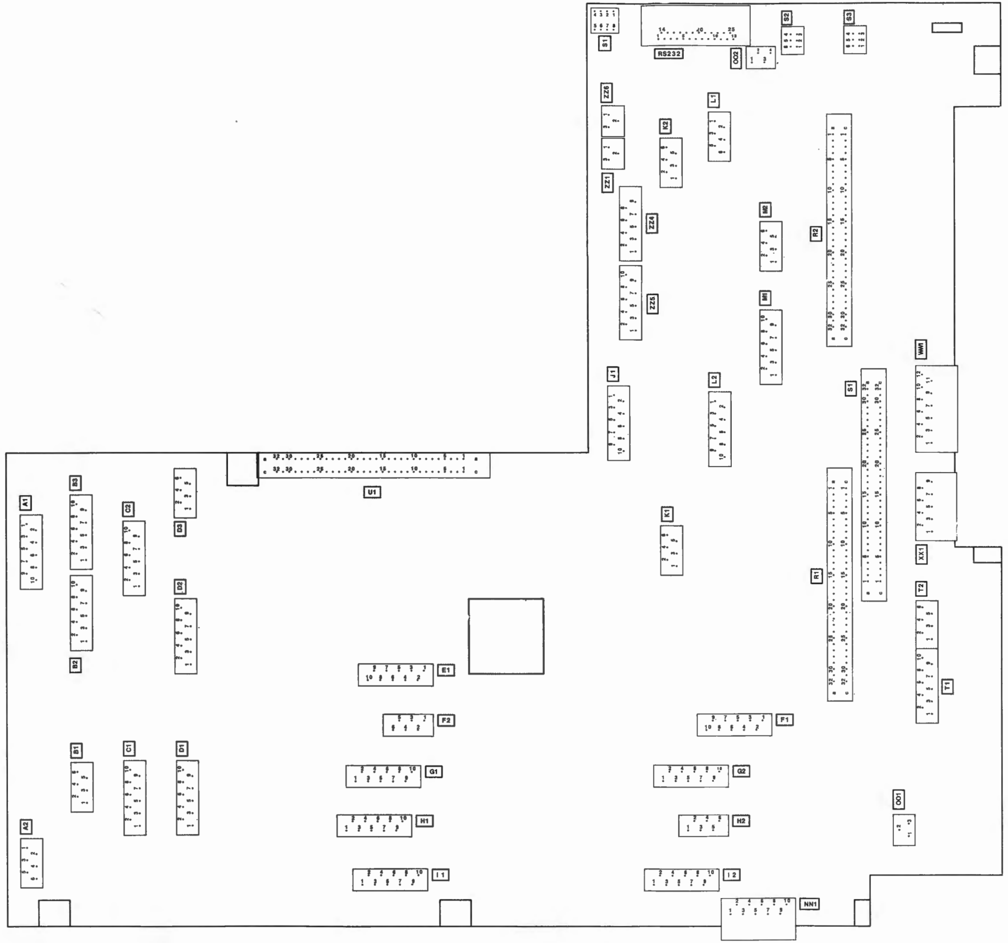
BC264	TO-92 VAR.4
BC327	TO-92 VAR.2
BC337	TO-92 VAR.2
BC368	TO-92 VAR.1
BC369	TO-92 VAR.1
BC375	TO-92 VAR.2
BC376	TO-92 VAR.2
BC546	TO-92 VAR.2
BC547	TO-92 VAR.2
BC548	TO-92 VAR.2
BC549	TO-92 VAR.2
BC556	TO-92 VAR.2
BC557	TO-92 VAR.2
BC558	TO-92 VAR.2
BC639	TO-92 VAR.1
BC640	TO-92 VAR.1
BC807	SOT-23 VAR.1
BC817	SOT-23 VAR.1
BC847	SOT-23 VAR.1
BC848	SOT-23 VAR.1
BC849	SOT-23 VAR.1
BC858	SOT-23 VAR.1
BC859	SOT-23 VAR.1
BD135	SOT-32 (TO-126)
BD434	SOT-32 (TO-126)
BD435	SOT-32 (TO-126)
BD436	SOT-32 (TO-126)
BD437	SOT-32 (TO-126)
BD438	SOT-32 (TO-126)
BFR30	SOT-23 VAR.3
BFR54	TO-92 VAR.2
BFS19	SOT-23 VAR.1
BF256	TO-92 VAR.4
BF450	TO-92 VAR.3
BF494	TO-92 VAR.3
BF992	SOT-143
BSD213	TO-72
BSV80	TO-18
BSW68	TO-39
BUT11F	SOT-186
BUW12	SOT-93
BUW85	SOT-82
BUX86	SOT-32 (TO-126)
PH2369	TO-92 VAR.2

Survey of modules
Modules A to Z
- Circuit diagram
- PCB lay-out
- Adjustments
- Electrical parts
Remote control

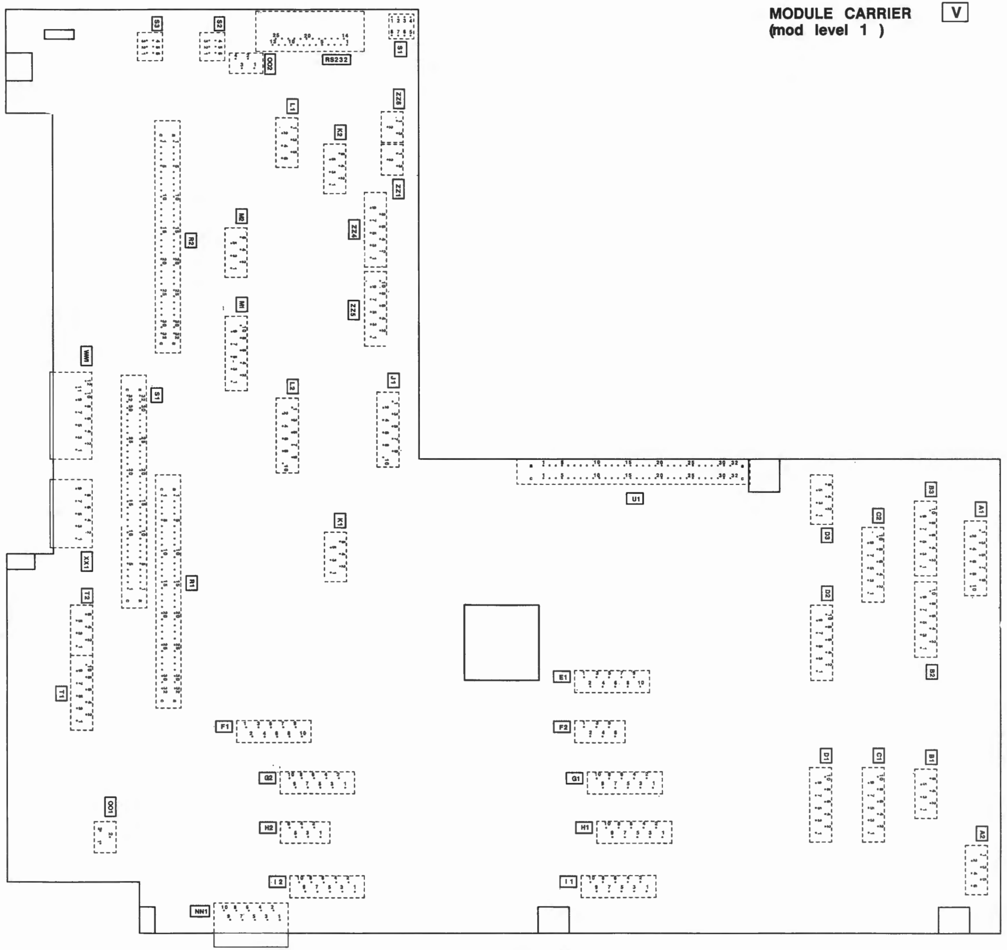
SURVEY OF MODULES VP415

MOD	DESCRIPTION
A	AUDIO PROCESSOR
B	RGB
C	VIDEO PROCESSOR
D	REF SOURCE
E	SLIDE DRIVE
F	MOTOR+SEQUENCE
G	GEN LOCK
H	ETBC B
I	ETBC C
J	FOCUS
K	HF PROCESSOR
L	VIDEO D.O.
M	RADIAL
N	DISPLAY KEYBOARD
P	FRONT LOADER
Q	RC5 MIRROR
R	DRIVE PROCESSOR
S	CONTROL
T	SUPPLY
U	ANALOG I/O
V	MODULE CARRIER
W	CPU DATAGR.
X	LV ROM
Y	VID MIX
Z	DECK ELECTRONICS

MODULE CARRIER V
(mod level 1)



COMPONENT SIDE



SOLDER SIDE

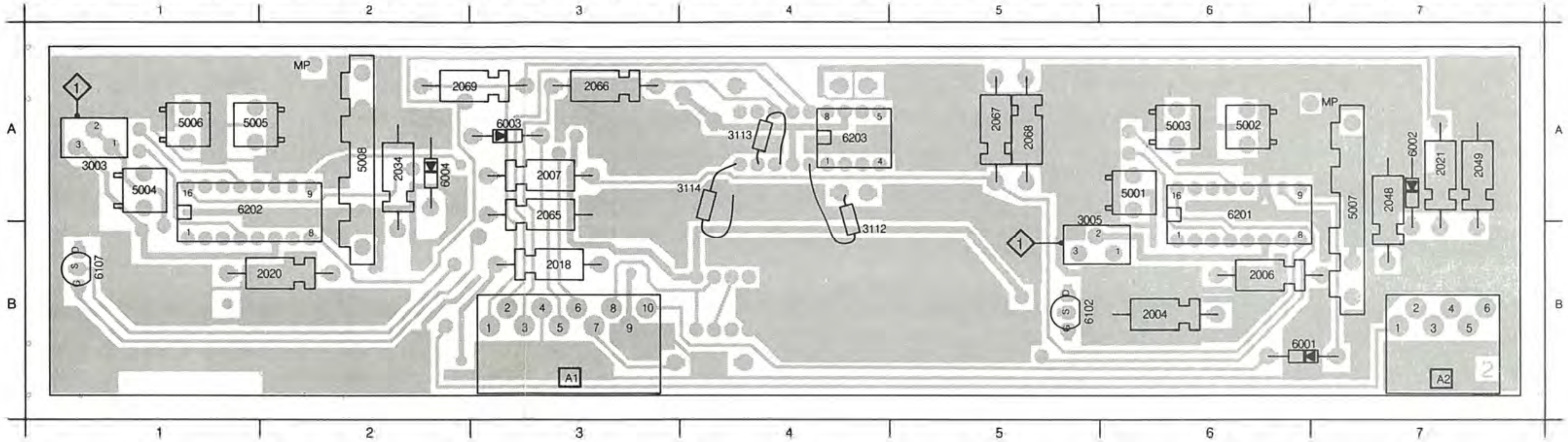
PCB. 01611
T03/720

CS 7 836

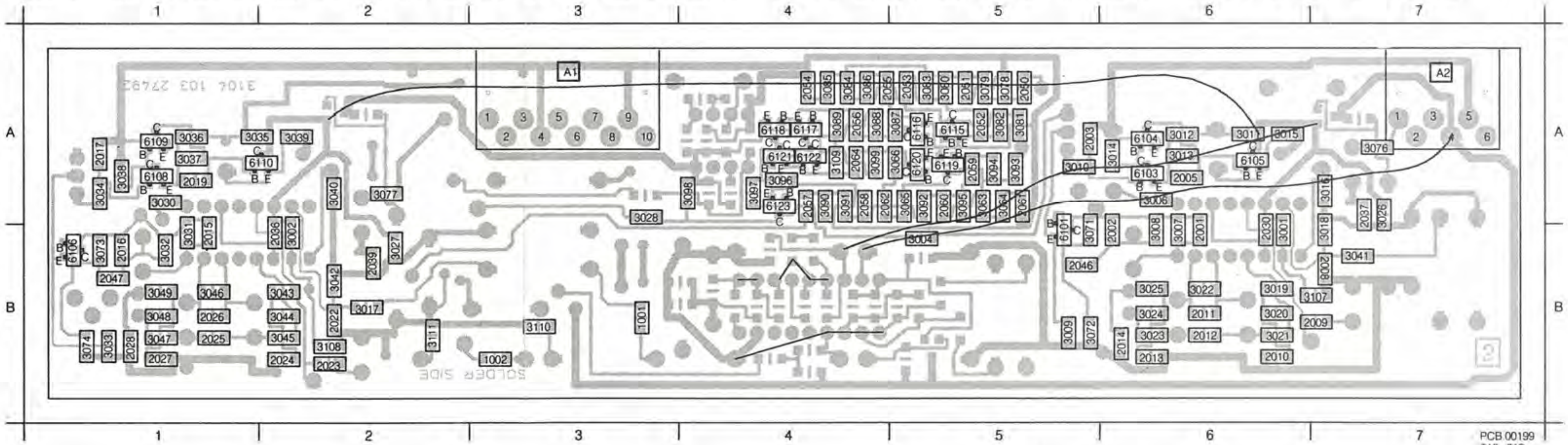
AUDIO PROC. MODULE [A]

(MOD LEVEL 2)

2004	B 6	2007	A 3	2020	B 1	2034	A 2	2049	A 7	2066	A 3	2068	A 5	3003	A 1	3112	B 4	3114	A 4	5002	A 6	5004	A 1	5006	A 1	5008	A 2	6002	A 7	6004	A 2	6107	B 1	6202	A 1
2006	B 6	2018	B 3	2021	A 7	2048	A 7	2065	A 3	2067	A 5	2069	A 2	3005	B 5	3113	A 4	5001	A 6	5003	A 6	5005	A 1	5007	A 7	6001	B 6	6003	A 3	6102	B 5	6201	A 6	6203	A 4



1001	B 3	2010	B 6	2019	A 1	2030	B 6	2052	A 5	2060	A 5	3007	B 6	3015	A 6	3023	B 6	3032	B 1	3040	A 2	3048	B 1	3073	B 1	3082	A 5	3090	A 4	3098	A 4	6103	A 6	6116	A 5
1002	B 3	2011	B 6	2022	B 2	2036	B 2	2053	A 5	2061	A 5	3008	B 6	3016	A 7	3024	B 6	3033	B 1	3041	B 7	3049	B 1	3074	B 1	3083	A 5	3091	A 4	3099	A 4	6104	A 6	6117	A 4
2001	B 6	2012	B 6	2023	B 2	2037	A 7	2054	A 4	2062	A 4	3009	B 5	3017	B 2	3025	B 6	3034	A 1	3042	B 2	3063	A 5	3076	A 7	3084	A 4	3092	A 5	3107	B 7	6105	A 6	6118	A 4
2002	B 6	2013	B 6	2024	B 2	2039	B 2	2055	A 4	2064	A 4	3010	A 5	3018	B 7	3026	A 7	3035	A 2	3043	B 2	3064	A 5	3077	A 2	3085	A 4	3093	A 5	3108	B 2	6106	B 1	6119	A 5
2003	A 5	2014	B 6	2025	B 1	2046	B 5	2056	A 4	3001	B 6	3011	A 6	3019	B 6	3027	B 2	3036	A 1	3044	B 2	3065	A 5	3078	A 5	3086	A 4	3094	A 5	3109	A 4	6108	A 1	6120	A 5
2005	A 6	2015	B 1	2026	B 1	2047	B 1	2057	A 4	3002	B 2	3012	A 6	3020	B 6	3028	A 3	3037	A 1	3045	B 2	3066	A 5	3079	A 5	3087	A 5	3095	A 5	3110	B 3	6109	A 1	6121	A 4
2008	B 7	2016	B 1	2027	B 1	2050	A 5	2058	A 4	3004	B 5	3013	A 6	3021	B 6	3030	A 1	3038	A 1	3046	B 1	3071	B 5	3080	A 5	3088	A 4	3096	A 4	3111	B 2	6110	A 2	6122	A 4
2009	B 7	2017	A 1	2028	B 1	2051	A 5	2059	A 5	3006	A 6	3014	A 6	3022	B 6	3031	B 1	3039	A 2	3047	B 1	3072	B 5	3081	A 5	3089	A 4	3097	A 4	6101	B 5	6115	A 5	6123	A 4



PCB 00199
T10 718

ADJUSTMENTS

Required
Test disc
Scope

Adjustment conditions
Load test disc
Normal play, picture no. 6200–6500 Audio 1,
6600–6900 Audio 2 (replay)
Audio modulation 1 kHz

Adjustments

1) **R3003, R3005** (Audio demod)

- Measure the output voltage on 1A1 and 3A1 (AUD2 and AUD1) with the scope.
- Adjust R3003 and R3005 until the output voltage is 1,8 Vpp.

Adjustment when item replaced:

replaced	**adjust**
IC6201	R3005
IC6202	R3003

LIST OF ELECTRICAL PARTS MODULE A

Filters

5007	4822 242 71658	SLC3251
5008	4822 242 71659	SLC3252

Coils

5001	4822 156 20928	8 mH
5002	4822 156 11009	130 µH
5003	4822 156 11009	130 µH
5004	4822 156 20928	8 mH
5005	4822 156 11008	110 µH
5006	4822 156 11008	110 µH

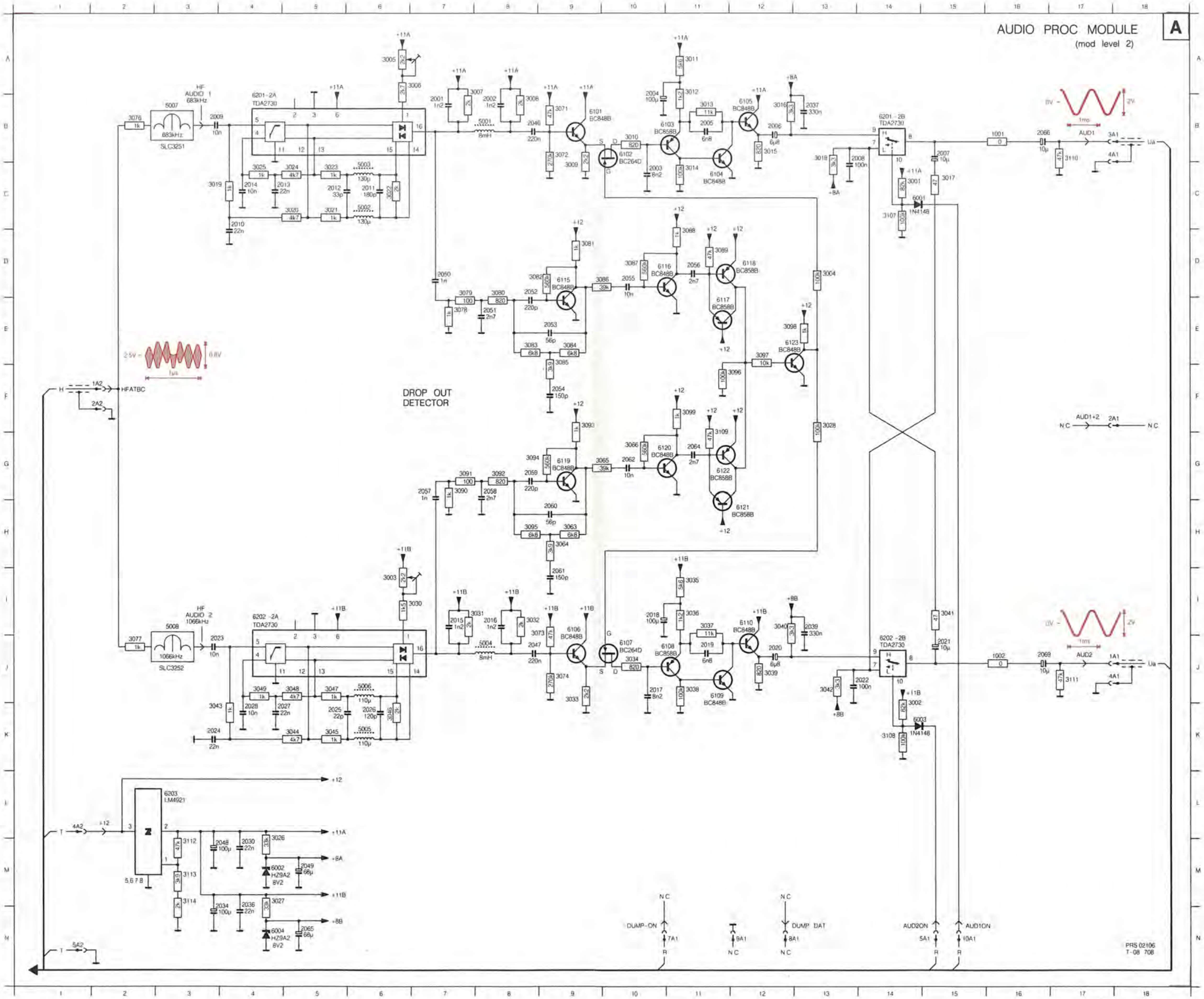
Potentiometers

3003	4822 100 11087	2.2 kΩ
3005	4822 100 11087	2.2 kΩ

2001	4822 122 32808	1.2 nF	
2002	4822 122 32808	1.2 nF	
2003	4822 122 32856	8.2 nF	
2004	5322 124 21711	100 µF	25 V
2005	4822 122 32597	6.8 nF	
2006	4822 124 22189	6.8 µF	63 V
2007	5322 124 21749	10 µF	63 V
2008	5322 122 32839	100 nF	
2009	4822 122 32442	10 nF	
2010	4822 122 31759	22 nF	
2011	4822 122 31768	180 pF	
2012	4822 122 32975	33 pF	
2013	4822 122 31759	22 nF	
2014	4822 122 32442	10 nF	
2015	4822 122 32808	1.2 nF	
2016	4822 122 32808	1.2 nF	
2017	4822 122 32856	8.2 nF	
2018	5322 124 21711	100 µF	25 V
2019	4822 122 32597	6.8 nF	
2020	4822 124 22189	6.8 µF	63 V
2021	5322 124 21749	10 µF	63 V
2022	5322 122 32839	100 nF	

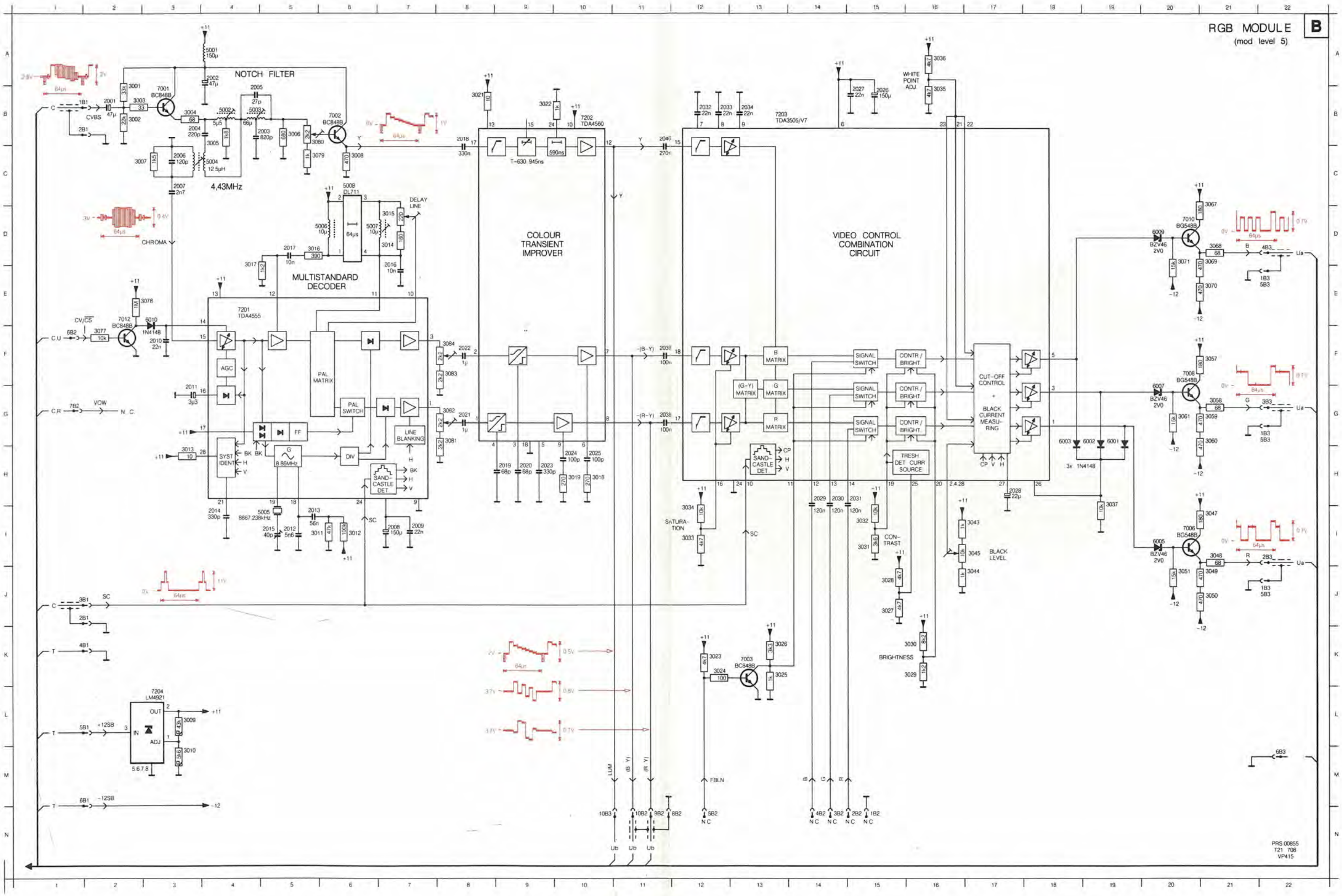
2023	4822 122 32442	10 nF	
2024	4822 122 31759	22 nF	
2025	4822 122 32482	22 pF	
2026	4822 122 31766	120 pF	
2027	4822 122 31759	22 nF	
2028	4822 122 32442	10 nF	
2030	4822 122 31759	22 nF	
2034	5322 124 21711	100 µF	25 V
2036	4822 122 31759	22 nF	
2037	4822 122 33007	330 nF	25 V
2039	4822 122 33007	330 nF	25 V
2046	4822 122 32927	220 nF	
2047	4822 122 32927	220 nF	
2048	5322 124 21711	100 µF	25 V
2049	5322 124 10512	68 µF	20% 16 V
2050	4822 122 32972	1 nF	
2051	4822 122 31783	2.7 nF	
2052	4822 122 31965	220 pF	
2053	4822 122 31774	56 pF	
2054	4822 122 31767	150 pF	
2055	4822 122 32442	10 nF	
2056	4822 122 31783	2.7 nF	

2057	5322 122 31647	1 nF	
2058	4822 122 31783	2.7 nF	
2059	4822 122 31965	220 pF	
2060	4822 122 31774	56 pF	
2061	4822 122 31767	150 pF	
2062	4822 122 32442	10 nF	
2064	4822 122 31783	2.7 nF	
2065	5322 124 10512	68 µF	20% 16 V
2066	5322 124 21749	10 µF	63 V
2069	5322 124 21749	10 µF	63 V



1001	B16
1002	J16
2001	B 7
2002	B 8
2003	C10
2004	A10
2005	B11
2006	B12
2007	B15
2008	B14
2009	B 3
2010	C 4
2011	C 6
2012	C 5
2013	C 5
2014	C 4
2015	I 7
2016	I 8
2017	J10
2018	I 10
2019	J11
2020	J12
2021	J15
2022	J14
2023	J 3
2024	K 3
2025	K 5
2026	K 6
2027	K 5
2028	K 4
2030	M 4
2034	M 4
2036	M 4
2037	B13
2039	I 13
2046	B 8
2047	J 8
2048	M 4
2049	M 5
2050	D 7
2051	E 8
2052	D 8
2053	E 9
2054	F 9
2055	D10
2056	D11
2057	G 7
2058	G 8
2059	G 8
2060	H 9
2061	I 9
2062	G10
2064	G11
2065	N 5
2066	B16
2069	J16
3001	C14
3002	J14
3003	I 6
3004	D13
3005	A 6
3006	A 7
3007	A 8
3008	B 8
3009	C 9
3010	B10
3011	A11
3012	A11
3013	B11
3014	C11
3015	B12
3016	B12
3017	C15
3018	B13
3019	C 3
3020	C 5
3021	C 5
3022	C 6
3023	C 5
3024	C 5
3025	C 4
3026	L 4
3027	M 4
3028	F13
3030	I 7
3031	I 8
3032	I 8
3033	J 9
3034	J10
3035	I 11
3036	I 11
3037	I 11
3038	J11
3039	J12
3040	I 12
3041	I 15
3042	J13
3043	K 3
3044	K 5
3045	K 5
3046	K 6
3047	J 5
3048	J 5
3049	J 4
3063	H 9
3064	H 9
3065	G10
3066	G10
3071	B 9
3072	B 9
3073	I 9
3074	J 9
3076	B 2
3077	J 2
3078	E 7
3079	D 7
3080	D 8
3081	D 9
3082	D 9
3083	E 8
3084	E 9
3085	E 9
3086	D10
3087	D10
3088	D11
3089	D11
3090	G 7
3091	G 7
3092	G 8
3093	F 9
3094	G 8
3095	H 8
3096	F12
3097	E12
3098	E12
3099	F11
3107	C14
3108	K14
3109	F11
3110	B17
3111	J17
3112	M 3
3113	M 3
3114	M 3
5001	B 8
5002	C 6
5003	C 6
5004	J 8
5005	K 6
5006	J 6
5007	B 3
5008	I 3
6001	C14
6002	M 4
6003	K14
6004	N 4
6101	B 9
6102	B10
6103	B11
6104	C11
6105	B12
6106	I 9
6107	J10
6108	J11
6109	J11
6110	I 12
6115	D 9
6116	D10
6117	E11
6118	D12
6119	G 9
6120	G10
6121	H12
6122	G11
6123	E12
6201	B 4
6201	B14
6202	I 4
6202	J14
6203	L 3

2001 B 2	2006 C 3	2011 G 3	2016 D 7	2021 G 8	2026 B15	2031 H15	2039 F11	3004 B 3	3009 L 3	3014 D 7	3019 H10	3025 K13	3030 K16	3035 B16	3045 I 17	3051 J20	3061 G20	3071 D20	3081 G 8	5002 B 4	5007 D 6	6005 I 20	7002 B 6	7012 E 2
2002 A 4	2007 C 3	2012 I 5	2017 D 5	2022 F 8	2027 B15	2032 B12	2040 B11	3005 B 4	3010 M 3	3015 D 7	3021 B 8	3026 K13	3031 I 15	3036 A16	3047 I 21	3057 F21	3067 C21	3077 F 2	3082 G 8	5003 B 4	5008 C 6	6007 G20	7003 K13	7201 E 4
2003 B 5	2008 I 7	2013 I 5	2018 B 8	2023 H 9	2028 H17	2033 B12	3001 B 2	3006 B 5	3011 I 6	3016 D 5	3022 B 9	3027 J15	3032 I 15	3037 H19	3048 I 21	3058 G21	3068 D21	3078 E 3	3083 F 8	5004 C 4	6001 G19	6009 D20	7006 I 20	7202 B10
2004 B 3	2009 I 7	2014 I 4	2019 H 9	2024 H10	2029 H14	2034 B13	3002 B 2	3007 C 3	3012 I 6	3017 D 4	3023 K12	3028 J15	3033 I 12	3043 I 17	3049 J21	3059 G21	3069 D21	3079 C 6	3084 F 8	5005 I 5	6002 G19	6010 E 3	7008 F20	7203 B13
2005 B 4	2010 F 3	2015 I 5	2020 H 9	2025 H10	2030 H14	2038 G11	3003 B 2	3008 C 6	3013 H 3	3018 H10	3024 K12	3029 K16	3034 I 12	3044 J17	3050 J21	3060 G21	3070 E21	3080 B 5	5001 A 4	5006 D 6	6003 G18	7001 B 3	7010 D20	7204 L 3



RGB MODULE B

(MOD LEVEL 5)

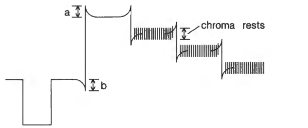
ADJUSTMENTS

Required
Test disc
Scope (dual beam) with X–deflection via B–channel
Or vector scope, if available

Adjustment conditions
Load test disc.
Still picture, colour pattern (picture no. 6200).

Adjustments

1) **L5002 and L5003** (notch filter)
- Using the scope, measure the luminance signal on 10B3, line triggered (see fig. B1)



LUMINANCE SIGNAL

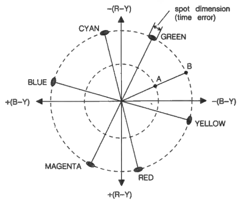
MDA.00585
T28/711

Fig. B1

- Adjust L5002 until the chroma rests in the luminance signal have disappeared.
- Adjust L5003 until overshoot a and undershoot b have the same amplitude.

2) **L5004** (Bandpass)
- Measure the chroma signal on 15–IC7201 with the scope.
- Adjust L5004 for minimum overshoots in the chroma signal.

3) **R3015 and L5007** (Delay line)
- Measure with the scope the (R–Y) signal at 9B2 with the A-channel and the (B–Y) signal on 10B2 with the B–channel,both AC coupled.
- Switch the scope to X–deflection and adjust it until the vector diagram below appears (see Fig. B2).



VECTOR DIAGRAM COLOUR BAR

MDA.00585
T28/711

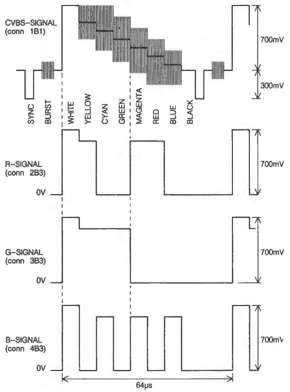
Fig. B2

The colour spots visible on the scope screen are lying at a certain distance B from origin O.
- Short–circuit pins 1–2 or 3–4 of delay line L5008. The spots in the vector diagram will lie closer to the origin now, at distance A from the origin. When the short–circuit is removed, the spots move outwards again (B).
- Adjust L5007 until the dimensions of the spots (in B) are minimal.
- Adjust R3015 until distance OB is twice distance OA in case of alternate short–circuiting of the delay line.

4) **C2015** (Oscillator frequency)

- Connect the scope as described sub 3).
- Short–circuit pins 1–2 or 3–4 of delay line L5008.
- Adjust C2015 until the dimensions of the colour spots of the vector diagram are minimal.

5) **R3080** (Luminance signal amplitude)
- Measure the G–signal on 3B3 (line freq.) with the scope . See fig. B3.



COLOUR BAR SIGNALS

Fig. B3

MDA.00586
T28/711

- Adjust R3080 for an average amplitude of 700 mV ± 7 mV.

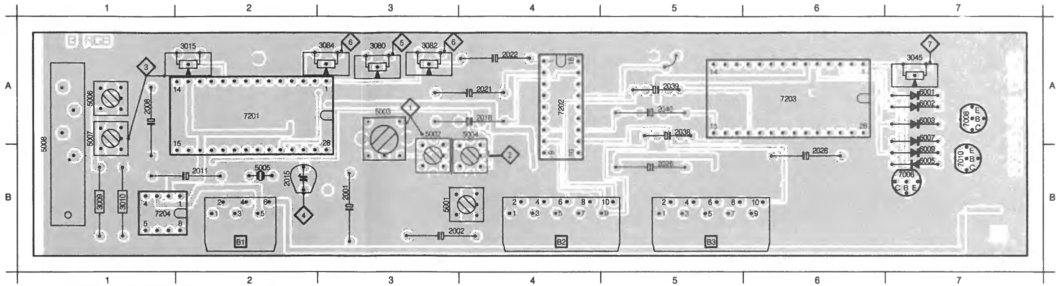
6) **R3082, R3084** (colour difference signal amplitude)
- Using the scope, measure the R–signal on 2B3 and adjust R3082 to the same amplitude of yellow, magenta and red.
- Using the scope, measure the B–signal on 4B3 and adjust R3084 to the same amplitude of cyan, magenta and blue (see Fig. B3).

7) **R3045** (black level)
- Measure output B-signal on 4B3 with the scope.
- Adjust R3045 for a black level of 0V ± 50 mV (see Fig. B3).

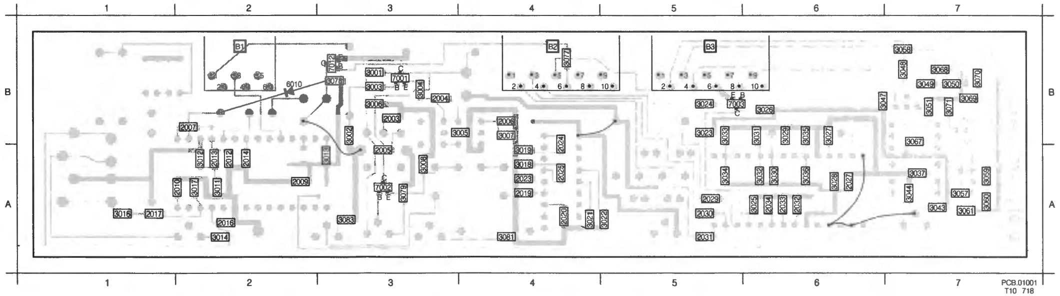
Adjustment when item replaced

replaced	**adjust**
IC7201	R3015, R3082, R3084, C2015, L5006, L5007
IC7202	R3080
IC7203	R3055, R3080, R3082, R3084
R3080	R3207)
R3082	R3305) on analog I/O module U
R3084	R3315)

	2008 A 1	2018 A 4	2026 B 5	2039 A 5	3010 B 1	3080 A 3	5001 B 3	5004 B 4	5007 A 1	6002 A 7	6007 A 7	7008 A 7	7202 A 4
2001 B 3	2011 B 2	2021 A 4	2028 B 6	2040 A 5	3015 A 2	3082 A 3	5002 B 3	5005 B 2	5008 A 1	6003 A 7	6009 B 7	7010 B 7	7203 A 6
2002 B 4	2015 B 2	2022 A 4	2038 A 5	3009 B 1	3045 A 7	3084 A 3	5003 B 3	5006 A 1	6001 A 7	6005 B 7	7006 B 7	7201 A 2	7204 B 1



2003 B 3	2009 A 2	2016 A 2	2024 A 4	2031 A 5	3002 A 3	3007 B 4	3013 A 3	3019 A 4	3025 A 6	3030 A 6	3035 A 6	3047 B 6	3057 A 7	3067 A 7	3077 B 4	6010 B 2
2004 B 3	2010 A 2	2017 A 1	2025 A 4	2032 A 6	3003 B 3	3008 A 3	3014 A 2	3021 A 4	3026 B 6	3031 A 6	3036 A 6	3048 B 7	3058 B 7	3068 B 7	3078 B 3	7001 B 3
2005 A 3	2012 A 2	2019 A 4	2027 A 6	2033 A 6	3004 B 3	3011 A 2	3016 A 1	3022 A 5	3027 A 6	3032 A 6	3037 A 7	3049 B 7	3059 A 7	3069 B 7	3079 A 3	7002 A 3
2006 B 4	2013 A 2	2020 A 4	2029 A 5	2034 A 6	3005 B 4	3012 A 2	3017 A 2	3023 B 5	3028 A 6	3033 A 5	3043 A 7	3050 B 7	3060 A 7	3070 B 7	3081 A 4	7003 B 5
2007 B 2	2014 A 2	2023 A 4	2030 A 5	3001 B 3	3006 B 3		3018 A 4	3024 B 5	3029 A 6	3034 A 5	3044 A 7	3051 B 7	3061 A 7	3071 B 7	3083 A 3	7012 B 3



PCB.01001
T10 718

LIST OF ELECTRICAL PARTS MODULE B

Crystals

5005	4822 242 70304	8.867238 MHz

Delay lines

5008	4822 320 40051	DL711

Coils

5001	4822 156 10993	150 μH
5002	4822 157 52873	5.5 μH
5003	4822 157 52875	66 μH
5004	4822 157 52874	12.5 μH
5006	4822 156 10995	10 μH
5007	5322 156 21341	10 μH

Potentiometers

3015	4822 100 10359	220 Ω
3045	5322 101 14066	10 kΩ
3080	5322 100 10117	2.2 kΩ
3082	5322 100 10117	2.2 kΩ
3084	5322 100 10117	2.2 kΩ

Trimcapacitors

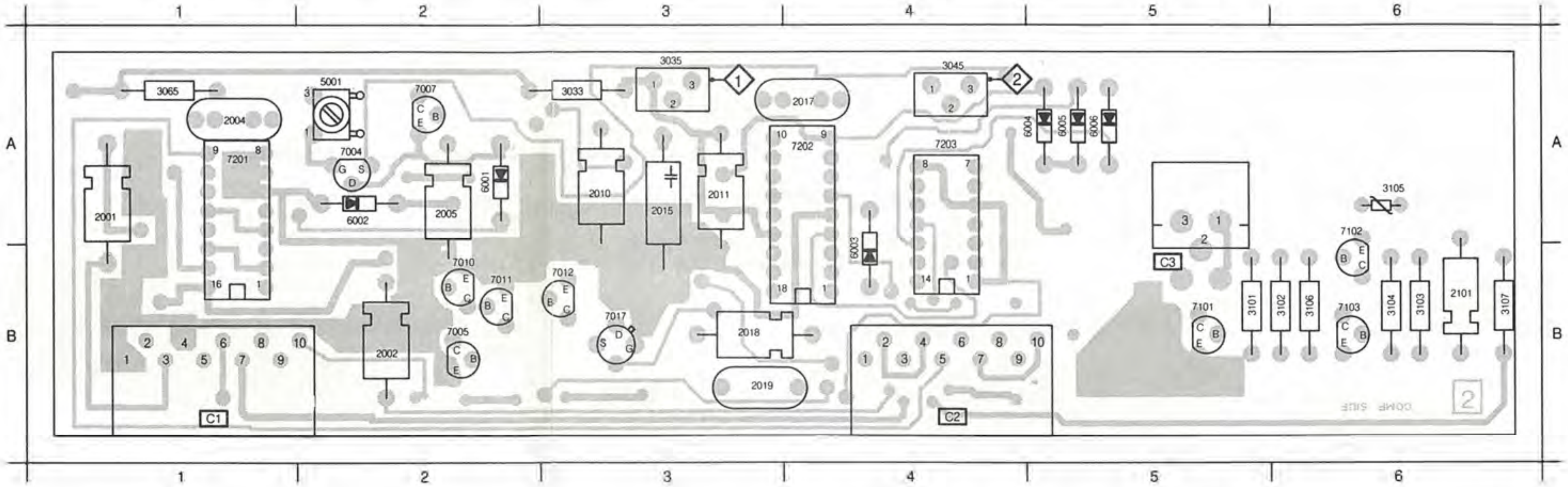
2015	4822 125 50092	40 pF

2001	4822 124 22027	47 μF	25 V
2002	4822 124 22027	47 μF	25 V
2003	4822 122 31974	820 pF	
2004	4822 122 31965	220 pF	
2005	4822 122 31966	27 pF	
2006	4822 122 31766	120 pF	
2007	4822 122 31783	2.7 nF	
2008	4822 124 22186	150 μF	25 V
2009	4822 122 31759	22 nF	
2010	4822 122 31759	22 nF	
2011	4822 124 22188	3.3 μF	63 V
2012	4822 122 31916	5.6 nF	
2013	4822 122 32183	56 nF	
2014	4822 121 42915	330 pF	
2015	4822 125 50092	40 pF	trimmer
2016	4822 122 32442	10 nF	
2017	4822 122 32442	10 nF	
2018	4822 121 41756	330 nF	10% 63 V
2019	4822 122 33002	68 pF	
2020	4822 122 33002	68 pF	
2021	4822 121 41719	1 μF	10% 100 V
2022	4822 121 41719	1 μF	10% 100 V
2023	4822 121 42915	330 pF	
2024	4822 122 32974	100 pF	
2025	4822 122 32974	100 pF	
2026	4822 124 22186	150 μF	25 V
2027	4822 122 31759	22 nF	
2028	5322 124 21643	22 μF	40 V
2029	4822 122 33008	120 nF	50 V
2030	4822 122 33008	120 nF	50 V
2031	4822 122 33008	120 nF	50 V
2032	4822 122 31759	22 nF	
2033	4822 122 31759	22 nF	
2034	4822 122 31759	22 nF	
2038	4822 121 41608	100 nF	100 V
2039	4822 121 41608	100 nF	100 V
2040	4822 121 41874	270 nF	63 V

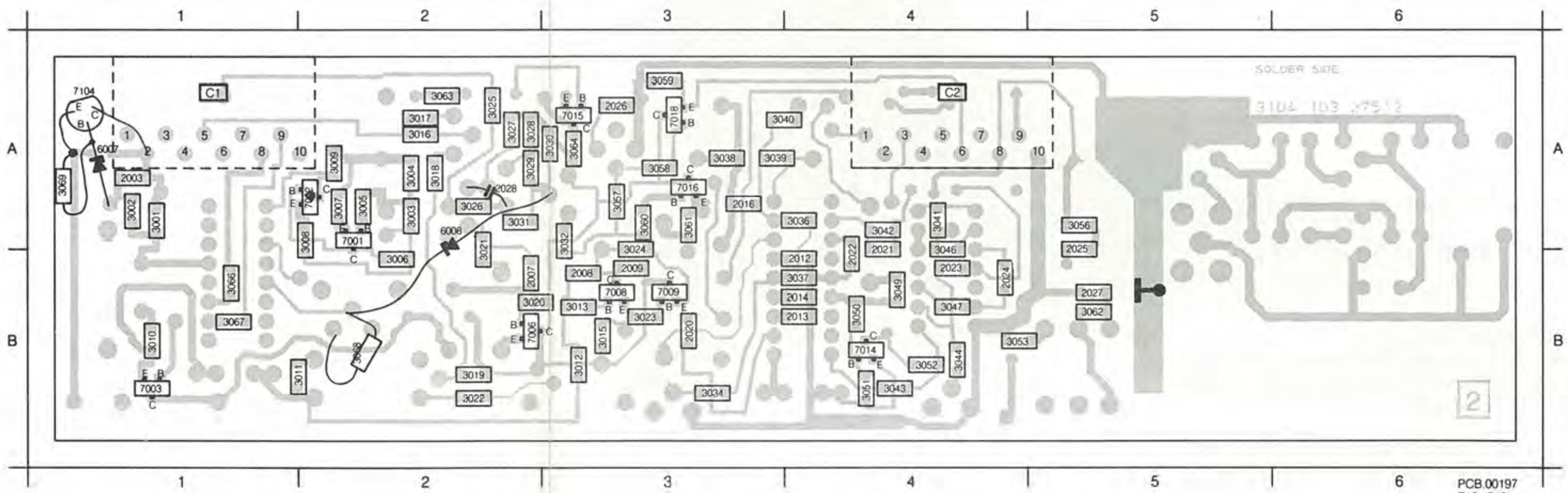
VIDEO PROC. MODULE C

(MOD LEVEL 3)

2001 A 1	2005 A 2	2017 A 4	3033 A 3	3065 A 1	6002 A 2	7005 B 2	7011 B 2	7201 A 1	2015 A 3	3102 B 6	3105 A 6	6004 A 5	7101 B 5
2002 B 2	2010 A 3	2018 B 3	3035 A 3	5001 A 2	6003 B 4	7007 A 2	7012 B 3	7202 A 4	2101 B 6	3103 B 6	3106 B 6	6005 A 5	7102 A 6
2004 A 1	2011 A 3	2019 B 3	3045 A 4	6001 A 2	7004 A 2	7010 B 2	7017 B 3	7203 A 4	3101 B 5	3104 B 6	3107 B 6	6006 A 5	7103 B 6



2003 A 1	2014 B 4	2024 B 4	3002 A 1	3008 A 2	3015 B 3	3021 B 2	3027 A 2	3034 B 3	3041 A 4	3049 B 4	3057 A 3	3063 A 2	6007 A 1	7008 B 3	7104 A 1
2007 B 2	2016 A 3	2025 A 5	3003 A 2	3009 A 2	3016 A 2	3022 B 2	3028 A 2	3036 A 4	3042 A 4	3050 B 4	3058 A 3	3064 A 3	6008 A 2	7009 B 3	
2008 B 3	2020 B 3	2026 A 3	3004 A 2	3010 B 1	3017 A 2	3023 B 3	3029 A 2	3037 B 4	3043 B 4	3051 B 4	3059 A 3	3066 B 1	7001 A 2	7014 B 4	
2009 B 3	2021 A 4	2027 B 5	3005 A 2	3011 B 1	3018 A 2	3024 A 3	3030 A 3	3038 A 3	3044 B 4	3052 B 4	3060 A 3	3067 B 1	7002 A 2	7015 A 3	
2012 B 4	2022 B 4	2028 A 2	3006 B 2	3012 B 3	3019 B 2	3025 A 2	3031 A 2	3039 A 3	3046 B 4	3053 B 4	3061 A 3	3068 B 2	7003 B 1	7016 A 3	
2013 B 4	2023 B 4	3001 A 1	3007 A 2	3013 B 3	3020 B 2	3026 A 2	3032 A 3	3040 A 3	3047 B 4	3056 A 5	3062 B 5	3069 A 1	7006 B 2	7018 A 3	



PCB 00197
T10 718

ADJUSTMENTS

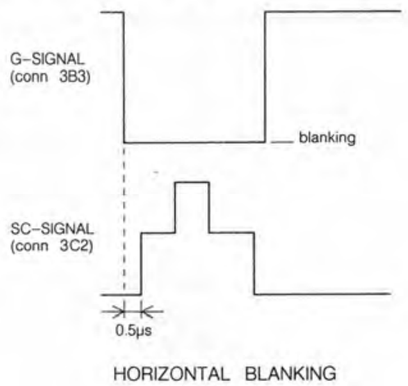
Required
Test disc
Voltmeter
Scope

Adjustment conditions
Load test disc
Still picture, colour bar (picture no. 6200).

Adjustments

1) **R3035** (frequency)
   - Measure the DC voltage on 18–IC7202.
   - Adjust R3035 for a DC voltage of 5.5V ± 0.5 V.

2) **R3045** (horizontal blanking)
   - Search for a white picture (e.g. picture no. 7500).
   - Measure sandcastle pulse SC on 3C2 with the scope (A–channel).
   - Measure the G–signal on 3B3 with the scope (B–channel) and trigger on this signal.
   - Adjust R3045 for a difference of 0,5μs between the SC and the G–signal (see Fig. C1).



MDA 00587
T28/711

Fig. C1

Adjustment when item replaced

replaced	**adjust**
IC7202	R3035, R3045
IC7203	R3045

LIST OF ELECTRICAL PARTS MODULE C

Coils

5001	4822 156 10992	117 μH

Potentiometers

3035	5322 101 10666	47 kΩ
3045	5322 101 10666	47 kΩ

NTC Resistors

3105	4822 116 30251	150 kΩ 0.5W

Fuse Resistors

3065	4822 111 10165	10 Ω
3108	4822 111 90357	33 Ω

NFR25 Resistors

3033	4822 111 30508	10 Ω
3107	4822 111 30593	3.3 Ω

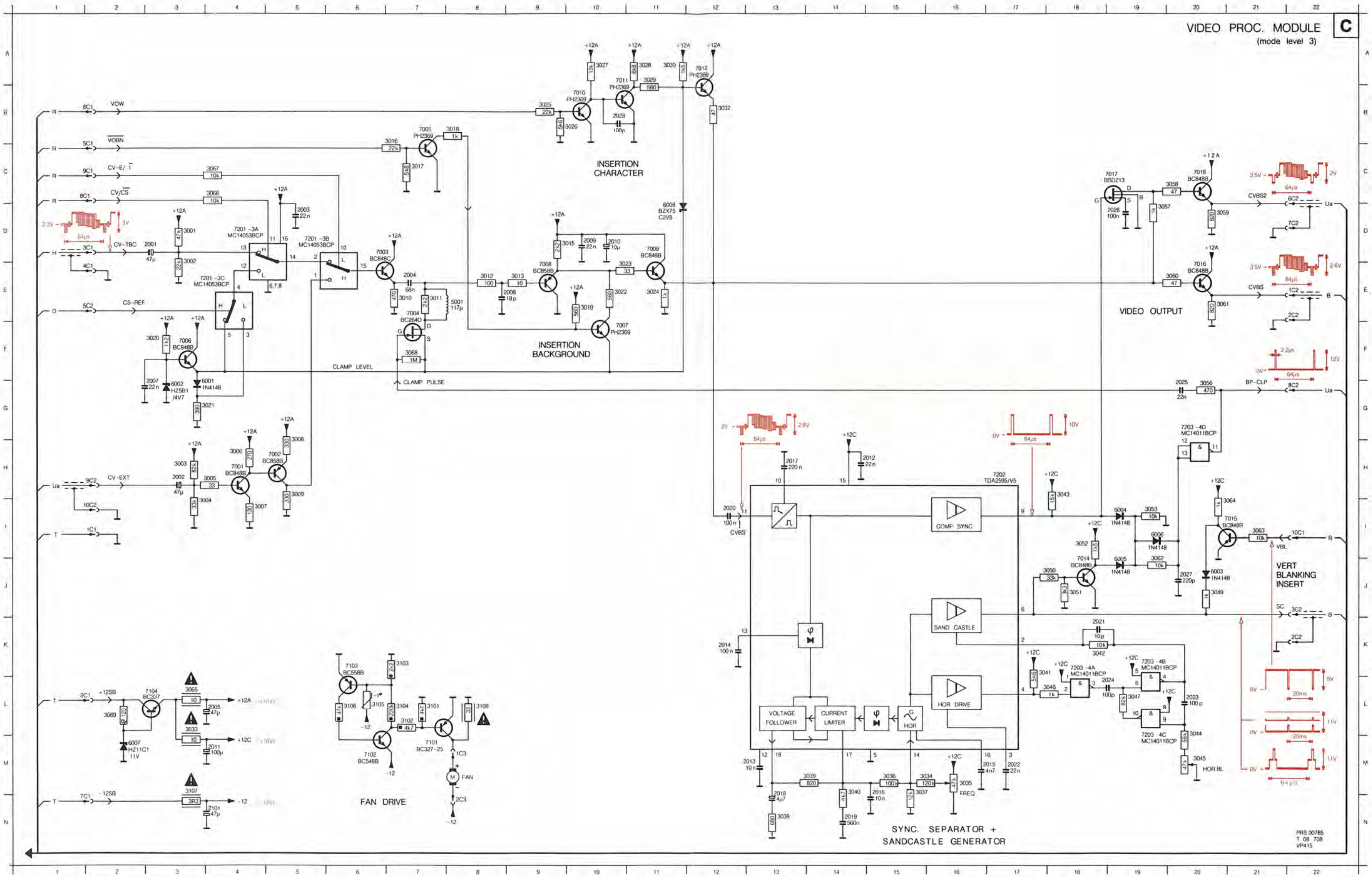
2001	4822 124 22027	47 μF	25 V
2002	4822 124 22027	47 μF	25 V
2003	4822 122 31759	22 nF	
2004	4822 121 42688	68 nF	100 V
2005	4822 124 22027	47 μF	25 V
2007	4822 122 31759	22 nF	
2008	4822 122 31769	18 pF	
2009	4822 122 31759	22 nF	
2010	5322 124 21749	10 μF	63 V
2011	5322 124 21711	100 μF	25 V
2012	4822 122 31759	22 nF	
2013	4822 122 32442	10 nF	
2014	5322 122 32839	100 nF	
2015	4822 121 51051	4.7 nF	63 V
2016	4822 122 32442	10 nF	
2017	4822 121 41876	220 nF	20% 63 V
2018	4822 124 22031	4.7 μF	63 V
2019	4822 121 41837	560 nF	20% 100 V
2020	5322 122 32839	100 nF	
2021	4822 122 31971	10 pF	
2022	4822 122 31759	22 nF	

2023	4822 122 32974	100 pF	
2024	4822 122 32974	100 pF	
2025	4822 122 31759	22 nF	
2026	5322 122 32839	100 nF	
2027	4822 122 31965	220 pF	
2028	4822 122 31316	100 pF	
2101	4822 124 22027	47 μF	25 V

2001	D 3	2008	E 9	2014	K12	2020	I 12	2026	D19	3003	H 3	3009	H 5	3016	B 7
2002	H 3	2009	D10	2015	M17	2021	K18	2027	J20	3004	I 4	3010	E 7	3017	C 7
2003	D 5	2010	D10	2016	M15	2022	M17	2028	B10	3005	H 4	3011	E 7	3018	B 8
2004	E 7	2011	M 4	2017	H13	2023	L20	2101	N 4	3006	H 4	3012	E 8	3019	E10
2005	L 4	2012	H15	2018	M13	2024	L19	3001	D 3	3007	I 4	3013	E 9	3020	F 3
2007	G 3	2013	M13	2019	N14	2025	G20	3002	D 3	3008	G 5	3015	D10	3021	G 4

3022	E10	3028	A11	3035	M16	3041	K18	3047	L19	3056	G20	3062	J19	3068	F 7
3023	E10	3029	A11	3036	M15	3042	K18	3049	I20	3057	D20	3063	I 21	3069	L 2
3024	E11	3030	A11	3037	M15	3043	H18	3050	J18	3058	C20	3064	I 21	3101	L 7
3025	B 9	3032	B12	3038	N13	3044	L20	3051	J18	3059	D20	3065	L 3	3102	L 7
3026	B10	3033	L 3	3039	M14	3045	M20	3052	I 18	3060	E20	3066	C 4	3103	K 7
3027	A10	3034	M16	3040	M14	3046	L18	3053	I 19	3061	E20	3067	C 4	3104	L 7

3105	L 6	6002	G 3	6008	D11	7006	F 3	7012	A12	7101	M 7	7201	E 4
3106	L 6	6003	J20	7001	H 4	7007	F10	7014	J18	7102	M 6	7202	H17
3107	M 3	6004	I 19	7002	H 5	7008	E 9	7015	I 21	7103	K 6	7203	K18
3108	L 8	6005	J19	7003	D 6	7009	D11	7016	E20	7104	L 3	7203	K19
5001	E 8	6006	I 19	7004	E 7	7010	B10	7017	C19	7201	D 4	7203	L19
6001	G 4	6007	M 2	7005	B 7	7011	A10	7018	C20	7201	D 5	7203	G20



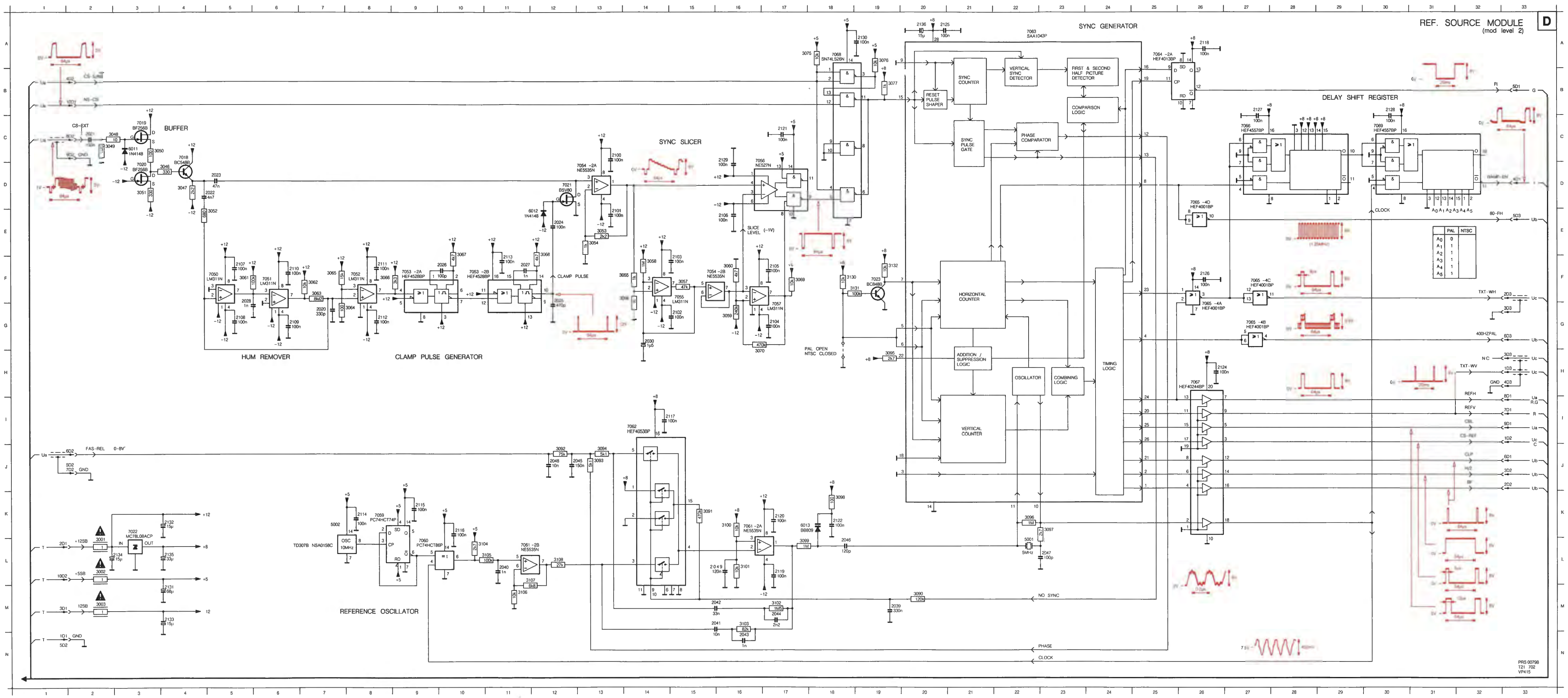
CS 6 869

2020	G 7	2024	E12	2028	F 5	2041	M16	2045	J13	2049	L16	2103	F15	2107	F 5	2111	F 8
2021	C 2	2025	F12	2030	G14	2042	M16	2046	L18	2100	C13	2104	G17	2108	G 5	2112	G 8
2022	D 5	2026	F10	2039	M19	2043	N16	2047	L23	2101	E13	2105	F17	2109	G 6	2113	F11
2023	D 5	2027	F11	2040	L11	2044	M17	2048	J12	2102	G15	2106	E16	2110	F 6	2114	K 8

2115	K 9	2119	L17	2124	H26	2128	B30	2132	K 4	2136	A20	3046	D 4	3050	C 4	3054	E13
2116	K10	2120	K17	2125	A20	2129	C16	2133	M 4	3001	L 2	3047	D 4	3051	D 3	3055	F14
2117	I 15	2121	C17	2126	F26	2130	A19	2134	L 3	3002	L 2	3048	C 3	3052	E 5	3056	F14
2118	A26	2122	K18	2127	B27	2131	M 4	2135	L 4	3003	M 2	3049	C 2	3053	E13	3057	F15

3058	F14	3062	F 7	3066	F 8	3070	H16	3090	M20	3094	J13	3098	K18	3102	M17	3106	M11
3059	G16	3063	F 7	3067	E10	3075	A18	3091	K15	3095	H19	3099	L17	3103	M16	3107	L11
3060	F16	3064	G 8	3068	E12	3076	A19	3092	J12	3096	K22	3100	K16	3104	L11	3108	L12
3061	F 5	3065	F 7	3069	F17	3077	B19	3093	J13	3097	K23	3101	L16	3105	L11	3130	F18

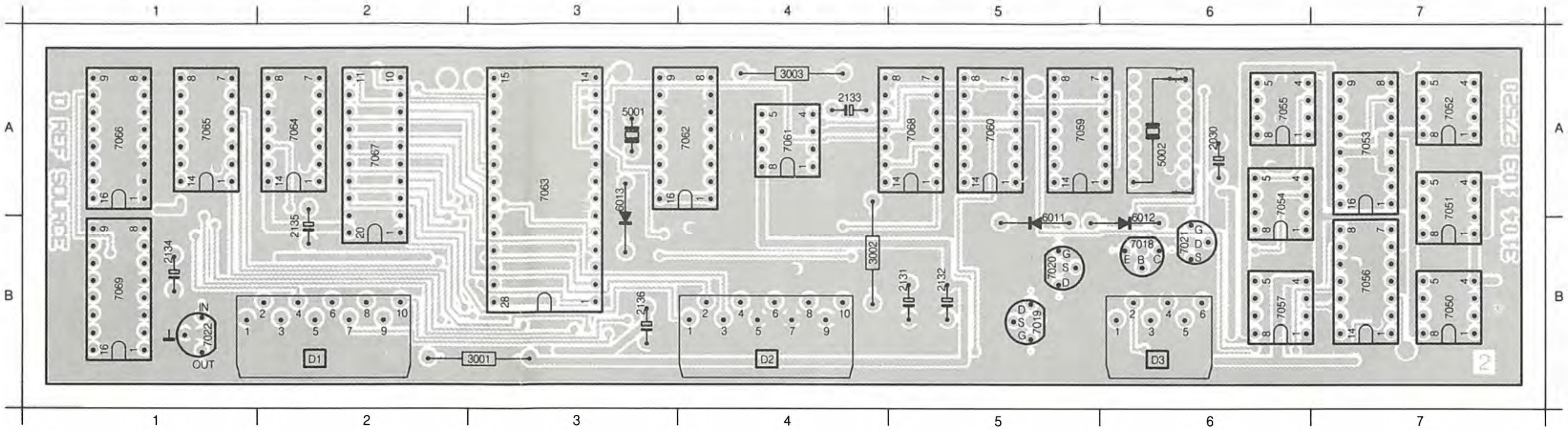
3131	F19	6011	C 3	7019	C 3	7023	F19	7053	F10	7055	F15	7060	L 9	7063	A22	7065	D26	7068	A18
3132	F19	6012	E12	7020	D 3	7050	F 5	7053	F 9	7056	C17	7061	L11	7064	A25	7065	F27	7069	C30
5001	L22	6013	K17	7021	D12	7051	F 6	7054	D13	7057	G17	7061	K16	7065	G26	7066	C27		
5002	K 7	7018	C 4	7022	K 3	7052	F 8	7054	F15	7059	K 8	7062	I 14	7065	G27	7067	H26		



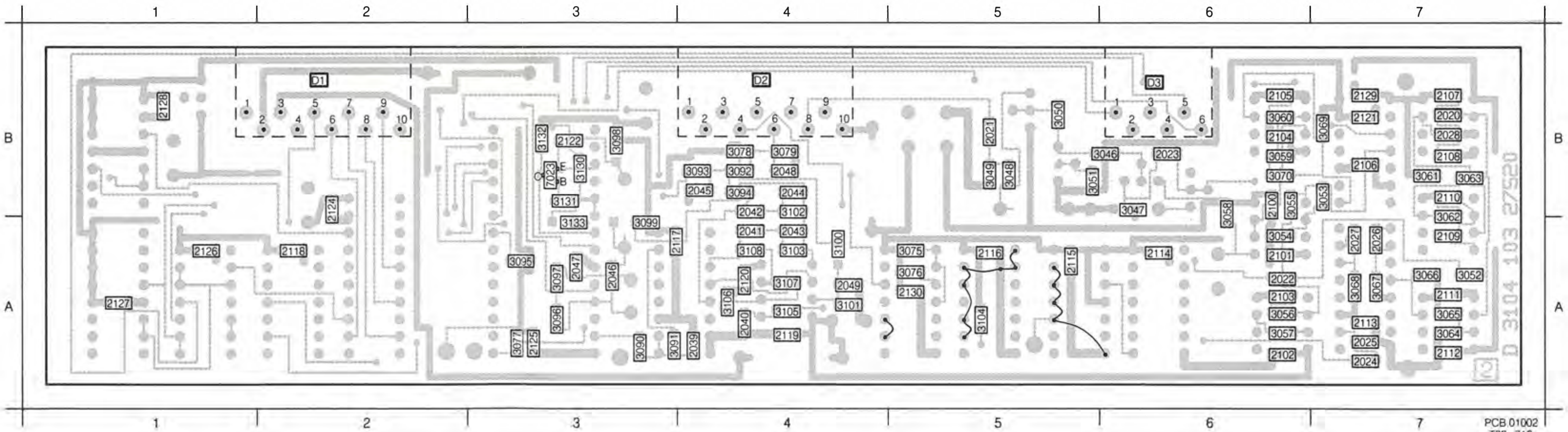
REF SOURCE MODULE D

(MOD LEVEL 2)

2030 A 6	2133 A 4	2136 B 3	3003 A 4	6011 B 5	7018 B 6	7021 B 6	7051 A 7	7054 A 6	7057 B 6	7061 A 4	7064 A 2	7067 A 2
2131 B 5	2134 B 1	3001 B 3	5001 A 3	6012 B 6	7019 B 5	7022 B 1	7052 A 7	7055 A 6	7059 A 5	7062 A 4	7065 A 1	7068 A 5
2132 B 5	2135 B 2	3002 B 4	5002 A 6	6013 A 3	7020 B 5	7050 B 7	7053 A 7	7056 B 7	7060 A 5	7063 A 3	7066 A 1	7069 B 1



2020 B 7	2026 A 7	2042 A 4	2048 B 4	2104 B 6	2110 B 7	2116 A 5	2122 B 3	2129 B 7	3050 B 5	3056 A 6	3062 A 7	3068 A 7	3078 B 4	3094 B 4	3100 A 4	3106 A 4	3133 A 3
2021 B 5	2027 A 7	2043 A 4	2049 A 4	2105 B 6	2111 A 7	2117 A 3	2124 A 2	2130 A 5	3051 B 5	3057 A 6	3063 B 7	3069 B 7	3079 B 4	3095 A 3	3101 A 4	3107 A 4	7023 B 3
2022 A 6	2028 B 7	2044 B 4	2100 A 6	2106 B 7	2112 A 7	2118 A 2	2125 A 3	3046 B 6	3052 A 7	3058 A 6	3064 A 7	3070 B 6	3090 A 3	3096 A 3	3102 A 4	3108 A 4	
2023 B 6	2039 A 4	2045 B 4	2101 A 6	2107 B 7	2113 A 7	2119 A 4	2126 A 1	3047 A 6	3053 A 7	3059 B 6	3065 A 7	3075 A 5	3091 A 3	3097 A 3	3103 A 4	3130 B 3	
2024 A 7	2040 A 4	2046 A 3	2102 A 6	2108 B 7	2114 A 6	2120 A 4	2127 A 1	3048 B 5	3054 A 6	3060 B 6	3066 A 7	3076 A 5	3092 B 4	3098 B 3	3104 A 5	3131 B 3	
2025 A 7	2041 A 4	2047 A 3	2103 A 6	2109 A 7	2115 A 5	2121 B 7	2128 B 1	3049 B 5	3055 A 6	3061 B 7	3067 A 7	3077 A 3	3093 B 4	3099 A 3	3105 A 4	3132 B 3	



PCB 01002
T03 712

LIST OF ELECTRICAL PARTS MODULE D

Crystals

5001	4822 242 70362	5 MHz
5002	4822 242 71664	10 MHz

NFR25 Resistors

3001	4822 111 30483	1 Ω
3002	4822 111 30483	1 Ω
3003	4822 111 30483	1 Ω

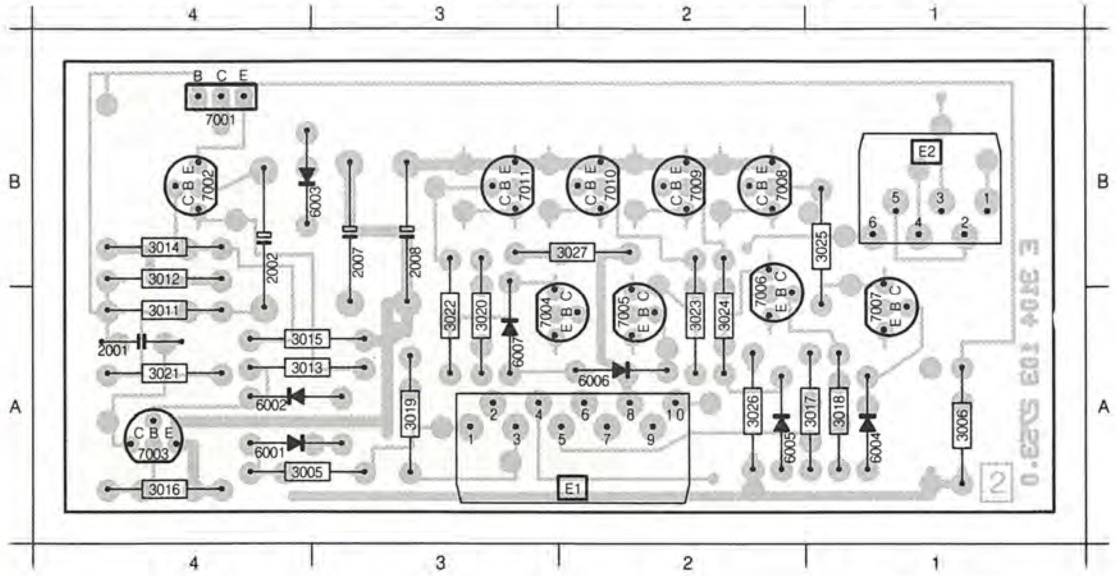
2020	4822 121 42915	330 pF	
2021	4822 122 33012	150 nF	50 V
2022	4822 122 31784	4.7 nF	
2023	4822 122 32542	47 nF	
2024	5322 122 32839	100 nF	
2025	4822 122 32976	470 pF	
2026	4822 122 32974	100 pF	
2027	4822 122 32972	1 nF	
2028	4822 122 32972	1 nF	
2030	4822 124 20942	1.5 µF	25 V
2039	4822 122 33007	330 nF	25 V
2040	4822 122 32972	1 nF	
2041	4822 122 32442	10 nF	
2042	5322 122 31848	33 nF	
2043	4822 122 32972	1 nF	
2044	4822 122 31644	2.2 nF	
2045	4822 122 33012	150 nF	50 V
2046	4822 122 31766	120 pF	
2047	4822 122 32974	100 pF	
2048	4822 122 32442	10 nF	
2049	4822 122 33008	120 nF	50 V
2100	5322 122 32839	100 nF	
2101	5322 122 32839	100 nF	
2102	5322 122 32839	100 nF	
2103	5322 122 32839	100 nF	
2104	5322 122 32839	100 nF	
2105	5322 122 32839	100 nF	
2106	5322 122 32839	100 nF	
2107	5322 122 32839	100 nF	
2108	5322 122 32839	100 nF	
2109	5322 122 32839	100 nF	
2110	5322 122 32839	100 nF	
2111	5322 122 32839	100 nF	
2112	5322 122 32839	100 nF	
2113	5322 122 32839	100 nF	
2114	5322 122 32839	100 nF	
2115	5322 122 32839	100 nF	
2116	5322 122 32839	100 nF	
2117	5322 122 32839	100 nF	
2118	5322 122 32839	100 nF	
2119	5322 122 32839	100 nF	
2120	5322 122 32839	100 nF	
2121	5322 122 32839	100 nF	
2122	5322 122 32839	100 nF	
2124	5322 122 32839	100 nF	
2125	5322 122 32839	100 nF	
2126	5322 122 32839	100 nF	
2127	5322 122 32839	100 nF	
2128	5322 122 32839	100 nF	
2129	5322 122 32839	100 nF	
2130	5322 122 32839	100 nF	
2131	5322 124 10455	68 µF	6.3 V
2132	4822 124 20977	15 µF	16 V
2133	4822 124 20977	15 µF	16 V
2134	4822 124 20977	15 µF	16 V
2135	4822 124 40963	33 µF	10 V
2136	4822 124 22191	15 µF	10 V

CS 7 840

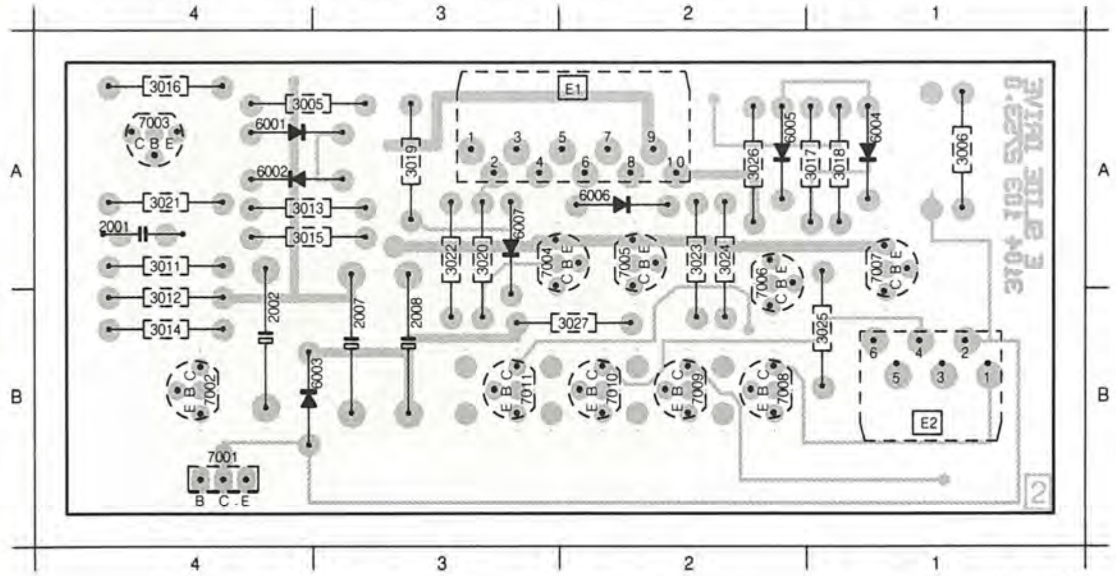
SLIDE DRIVE MODULE E

(MOD LEVEL 3)

2001 A 4	3006 A 1	3015 A 4	3020 A 3	3025 B 1	6003 B 3	7001 B 4	7006 A 2	7011 B 3
2002 A 4	3011 A 4	3016 A 4	3021 A 4	3026 A 2	6004 A 1	7002 B 4	7007 A 1	
2007 A 3	3012 A 4	3017 A 1	3022 A 3	3027 B 3	6005 A 2	7003 A 4	7008 B 2	
2008 A 3	3013 A 4	3018 A 1	3023 A 2	6001 A 4	6006 A 3	7004 A 3	7009 B 2	
3005 A 4	3014 B 4	3019 A 3	3024 A 2	6002 A 4	6007 A 3	7005 A 2	7010 B 2	



2001 A 4	3006 A 1	3015 A 4	3020 A 3	3025 B 1	6003 B 3	7001 B 4	7006 A 2	7011 B 3
2002 B 4	3011 A 4	3016 A 4	3021 A 4	3026 A 2	6004 A 1	7002 B 4	7007 A 1	
2007 B 3	3012 B 4	3017 A 1	3022 A 3	3027 B 3	6005 A 2	7003 A 4	7008 B 2	
2008 B 3	3013 A 4	3018 A 1	3023 A 2	6001 A 4	6006 A 3	7004 A 3	7009 B 2	
3005 A 4	3014 B 4	3019 A 3	3024 A 2	6002 A 4	6007 A 3	7005 A 2	7010 B 2	



PCB 01000
T03/716

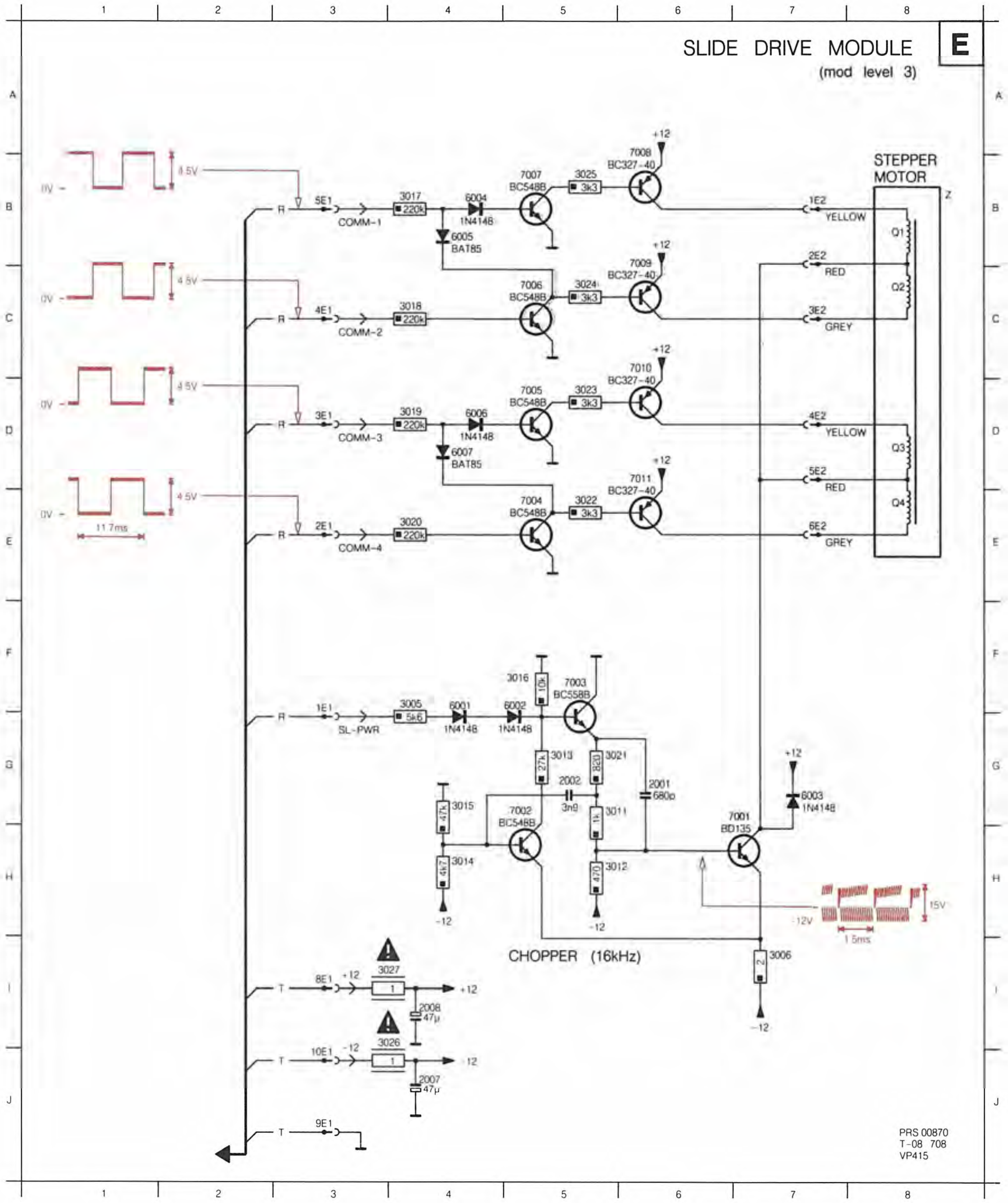
LIST OF ELECTRICAL PARTS MODULE E

NFR25 Resistors

3026	4822 111 30483	1 Ω
3027	4822 111 30483	1 Ω

2001	4822 122 30053	680 pF	100 V
2002	4822 121 50959	3.9 nF	63 V
2007	4822 124 22027	47 µF	25 V
2008	4822 124 22027	47 µF	25 V

2001	G 6	3006	I 7	3015	G 4	3020	E 4	3025	B 5	6003	G 7	7001	G 7	7006	C 5	7011	D 6
2002	G 5	3011	G 6	3016	F 5	3021	G 6	3026	I 4	6004	B 4	7002	G 5	7007	B 5	Q1	B 8
2007	J 4	3012	H 6	3017	B 4	3022	E 5	3027	I 4	6005	B 4	7003	F 5	7008	A 6	Q2	C 8
2008	I 4	3013	G 5	3018	C 4	3023	D 5	6001	F 4	6006	D 4	7004	E 5	7009	B 6	Q3	D 8
3005	F 4	3014	H 4	3019	D 4	3024	C 5	6002	F 5	6007	D 4	7005	D 5	7010	C 6	Q4	E 8



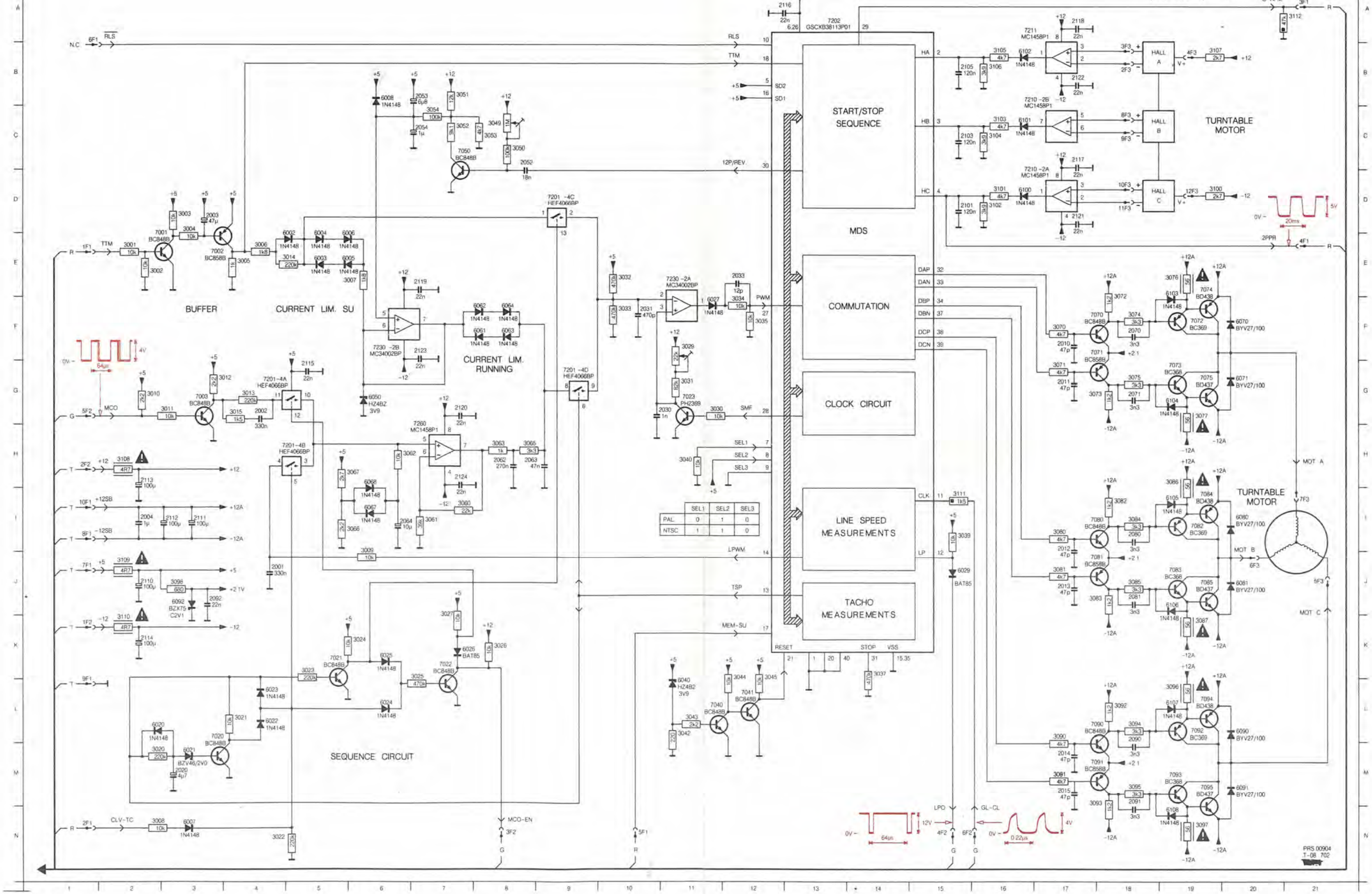
2001	J 4	2015	M17	2063	H 8	2101	D15	2116	A13	3001	E 2	3010	G 2	3023	K 5
2002	G 4	2020	M 3	2064	I 6	2103	C15	2117	C17	3002	E 2	3011	G 3	3024	K 6
2003	D 3	2030	G11	2070	F18	2105	B15	2118	A17	3003	D 3	3012	G 4	3025	K 7
2004	I 2	2031	F10	2071	G18	2110	J 2	2119	E 7	3004	D 3	3013	G 4	3026	K 8
2010	F17	2033	E12	2080	I 18	2111	I 3	2120	G 7	3005	E 4	3014	E 5	3027	J 7
2011	G17	2052	C 8	2081	J18	2112	I 3	2121	D17	3006	E 4	3015	G 4	3029	F11
2012	I 17	2053	B 7	2090	L18	2113	H 2	2122	B17	3007	E 6	3020	M 2	3030	G11
2013	J17	2054	C 7	2091	M18	2114	K 2	2123	F 7	3008	N 2	3021	L 4	3031	G11
2014	M17	2062	H 8	2092	J 3	2115	G 5	2124	H 7	3009	I 6	3022	N 4	3032	E10

3033	F10	3045	K12	3062	H 7	3074	F18	3084	I 18	3095	M18	3105	B16	6003	E 5
3034	F12	3049	C 8	3063	H 8	3075	G18	3085	J18	3096	L19	3106	B16	6004	E 5
3035	F12	3050	C 8	3065	H 8	3076	E19	3086	H19	3097	N19	3107	B19	6005	E 6
3037	K14	3051	B 7	3066	I 6	3077	G19	3087	K19	3098	J 3	3108	H 2	6006	E 6
3039	I 15	3052	C 7	3067	H 6	3080	I 17	3090	L17	3100	D19	3109	J 2	6007	N 3
3040	H11	3053	C 8	3070	F17	3081	J17	3091	M17	3101	D16	3110	K 2	6008	B 6
3042	L11	3054	C 7	3071	G17	3081	M17	3092	L18	3102	D16	3111	I 15	6020	L 2
3043	L11	3060	I 7	3072	E18	3082	I 18	3093	M18	3103	C16	3112	A21	6021	M 3
3044	K12	3061	I 7	3073	G18	3083	J18	3094	L18	3104	C16	6002	E 5	6022	L 4

6023	L 4	6062	F 8	6090	L20	6106	J19	7023	G11	7075	G19	7092	L19	7210	B16
6024	L 6	6063	F 8	6091	M20	6107	L19	7040	L11	7080	I 18	7093	M19	7210	C16
6025	K 6	6064	F 8	6092	J 3	6108	N19	7041	L12	7081	J18	7094	L19	7211	A16
6026	K 7	6067	I 6	6100	D16	7001	D 3	7050	C 7	7082	I 19	7095	M19	7230	F 6
6027	F11	6068	H 6	6101	C16	7002	E 3	7070	F18	7083	J19	7201	D 9	7230	E11
6029	J15	6070	F20	6102	B16	7003	G 3	7071	F18	7084	I 19	7201	G 9	7260	G 7
6040	L11	6071	G20	6103	E19	7020	L 3	7072	F19	7085	J19	7201	G 4		
6050	G 6	6080	I 20	6104	G19	7021	K 5	7073	G19	7090	L18	7201	H 5		
6061	F 8	6081	J20	6105	I 19	7022	K 7	7074	E19	7091	M18	7202	A13		

MOTOR+SEQUENCE MODULE F

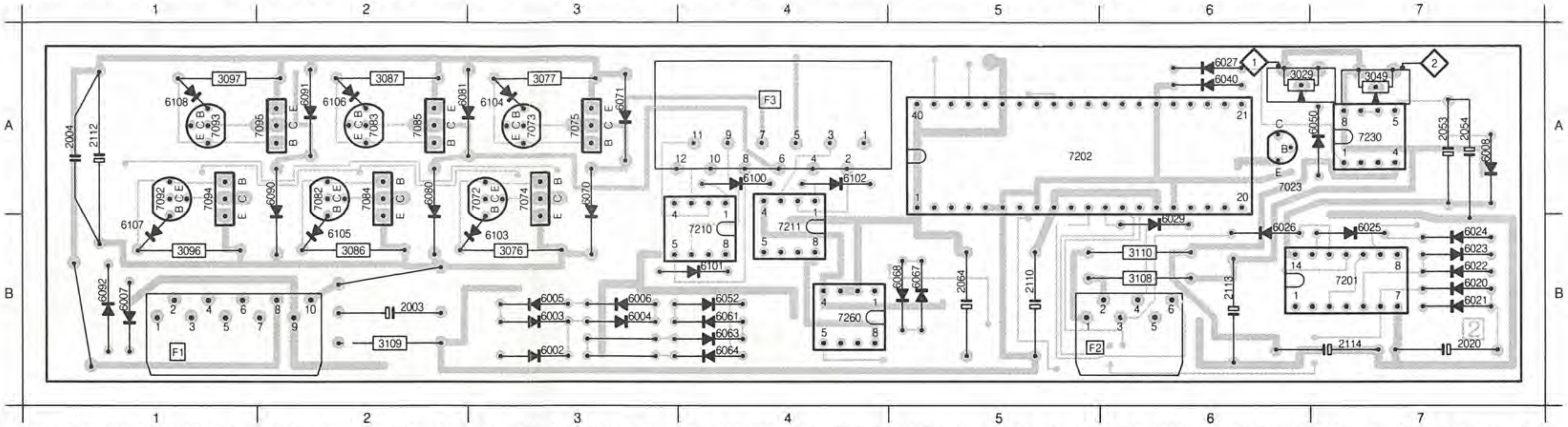
(mod level 5)



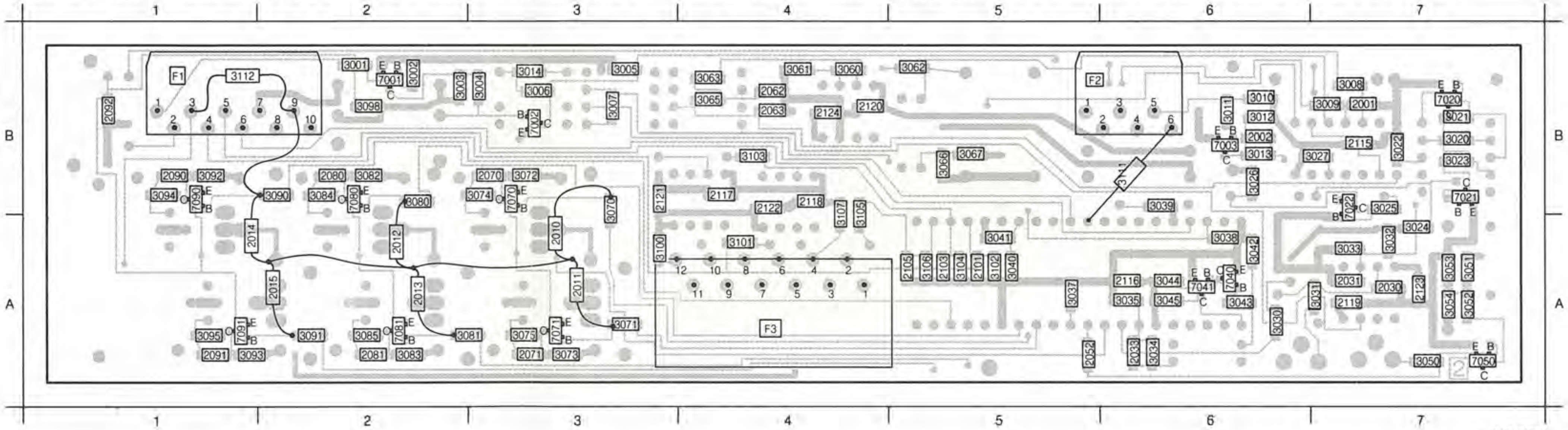
MOTOR + SEQUENCE MODULE F

(MOD. LEVEL 5)

1002 B 6	2054 A 7	2114 B 7	3086 B 2	3109 B 2	6004 B 3	6106 A 2	6020 B 7	6025 B 7	6050 A 7	6067 B 5	6081 A 2	6101 B 4	7074 A 3	7085 A 2	7201 B 7	7260 B 4
2003 B 2	2064 B 5	3029 A 6	3087 A 2	3110 B 6	6104 A 3	6007 B 1	6021 B 7	6026 B 6	6052 B 4	6068 B 5	6090 A 2	6102 A 4	7075 A 3	7092 A 1	7202 A 5	
2004 A 1	2110 B 5	3049 A 7	3096 B 1	6002 B 3	6005 B 3	6107 B 1	6022 B 7	6027 A 6	6061 B 4	6070 A 3	6091 A 2	7023 A 6	7082 A 2	7093 A 1	7210 B 4	
2020 B 7	2112 A 1	3076 B 3	3097 A 1	6003 B 3	6105 B 2	6008 A 7	6023 B 7	6029 B 6	6063 B 4	6071 A 3	6092 B 1	7072 A 3	7083 A 2	7094 A 1	7211 B 4	
2053 A 7	2113 B 6	3077 A 3	3108 B 6	6103 B 3	6006 B 3	6108 A 1	6024 B 7	6040 A 6	6064 B 4	6080 A 2	6100 A 4	7073 A 3	7084 A 2	7095 A 2	7230 A 7	



2001 B 7	2015 A 2	2070 B 3	2101 A 5	2119 A 7	3002 B 2	3009 B 7	3014 B 3	3026 B 6	3035 A 6	3043 A 6	3054 A 7	3067 B 5	3080 B 2	3091 A 2	3101 A 4	7001 B 2	7041 A 6	7091 A 1
2002 B 6	2030 A 7	2071 A 3	2103 A 5	2120 B 4	3003 B 2	3010 B 6	3020 B 7	3027 B 7	3037 A 5	3044 A 6	3060 B 4	3070 A 3	3081 A 3	3092 B 1	3102 A 5	7002 B 3	7050 A 7	
2010 A 3	2031 A 7	2080 B 2	2105 A 5	2121 A 3	3004 B 3	3011 B 6	3021 B 7	3030 A 6	3038 A 6	3045 A 6	3061 B 4	3071 A 3	3082 B 2	3093 A 1	3103 B 4	7003 B 6	7070 A 3	
2011 A 3	2033 A 6	2081 A 2	2115 B 7	2122 A 4	3005 B 3	3111 B 6	3022 B 7	3031 A 7	3039 B 6	3050 A 7	3062 B 5	3072 B 3	3083 A 2	3094 B 1	3104 A 5	7020 B 7	7071 A 3	
2012 A 2	2052 A 5	2090 B 1	2116 A 6	2123 A 7	3006 B 3	3012 B 6	3023 B 7	3032 A 7	3040 A 5	3051 A 7	3063 B 4	3073 A 3	3084 B 2	3095 A 1	3105 A 4	7021 B 7	7080 A 2	
2013 A 2	2062 B 4	2091 A 1	2117 B 4	2124 B 4	3007 B 3	3112 B 1	3024 A 7	3033 A 7	3041 A 5	3052 A 7	3065 B 4	3074 B 3	3085 A 2	3098 B 2	3106 A 5	7022 A 7	7081 A 2	
2014 A 1	2063 B 4	2092 B 1	2118 B 4	3001 B 2	3008 B 7	3013 B 6	3025 A 7	3034 A 6	3042 A 6	3053 A 7	3066 B 5	3075 A 3	3090 B 2	3100 A 3	3107 A 4	7040 A 6	7090 A 1	



PCB.01003
T03/718

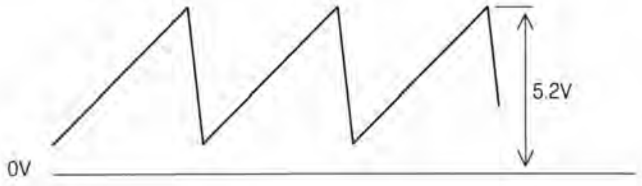
ADJUSTMENTS

Required
Test disc
Scope
Voltmeter

Adjustment conditions
Rotating disc

Adjustment

1) **R3029** (sawtooth signal)
   - Measure the sawtooth signal on 3–IC7230–2A (see fig. F1).



SAWTOOTH SIGNAL

Fig. F1

MDA.00587
T28/711

   - Adjust R3029 for a peak amplitude of 5.2V ± 0.1 V.

2) **R3049** (current limiter)
   - Measure the DC voltage on 7–IC7230 and adjust R3049 until this voltage is 3.2V ± 0.1V.

Adjustment when item replaced

replaced	**adjust**
IC7230	R3029, R3049

LIST OF ELECTRICAL PARTS MODULE F

Potentiometers

3029	5322 101 10574	22 kΩ
3049	4822 101 10755	1 MΩ

Fuse Resistors

3076	4822 111 30848	56 Ω
3077	4822 111 30848	56 Ω
3086	4822 111 30848	56 Ω
3087	4822 111 30848	56 Ω
3096	4822 111 30848	56 Ω
3097	4822 111 30848	56 Ω
3108	5322 111 90376	4.7 Ω
3109	5322 111 90376	4.7 Ω
3110	5322 111 90376	4.7 Ω

2001	4822 122 33007	330 nF	25 V
2002	4822 122 33007	330 nF	25 V
2003	4822 124 22027	47 µF	25 V
2004	4822 121 41719	1 µF	10% 100 V
2010	4822 122 31772	47 pF	
2011	4822 122 31772	47 pF	
2012	4822 122 31772	47 pF	
2013	4822 122 31772	47 pF	
2014	4822 122 31772	47 pF	
2015	4822 122 31772	47 pF	
2020	4822 124 22031	4.7 µF	63 V
2034	4822 122 32442	10 nF	
2035	4822 122 32856	8.2 nF	
2036	4822 122 32566	3.9 nF	
2037	4822 122 32442	10 nF	
2038	4822 122 31644	2.2 nF	
2039	4822 122 32442	10 nF	
2040	4822 122 31969	3.3 nF	
2041	4822 122 32442	10 nF	
2042	4822 122 31969	3.3 nF	
2043	5322 124 21643	22 µF	40 V
2044	4822 122 32974	100 pF	

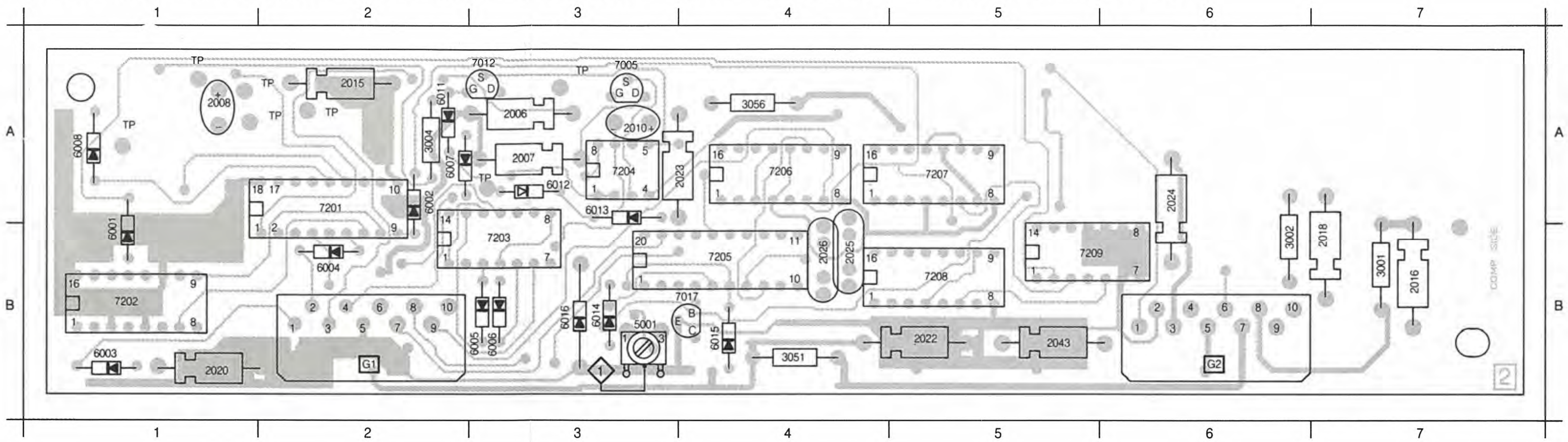
2030	5322 122 31647	1 nF	
2031	4822 122 32976	470 pF	
2033	4822 122 32139	12 pF	
2052	4822 122 31759	18 nF	
2053	4822 124 22189	6.8 µF	63 V
2054	4822 124 22028	1 µF	63 V
2062	4822 122 33009	270 nF	25 V
2063	4822 122 32542	47 nF	
2064	5322 124 21749	10 µF	63 V
2070	4822 122 31969	3.3 nF	
2071	4822 122 31969	3.3 nF	
2080	4822 122 31969	3.3 nF	
2081	4822 122 31969	3.3 nF	
2090	4822 122 31969	3.3 nF	
2091	4822 122 31969	3.3 nF	
2092	4822 122 31759	22 nF	
2101	4822 122 33008	120 nF	50 V
2103	4822 122 33008	120 nF	50 V
2105	4822 122 33008	120 nF	50 V
2110	5322 124 21711	100 µF	25 V
2111	5322 124 21711	100 µF	25 V
2112	4822 124 22221	100 µF	63 V

2113	5322 124 21711	100 µF	25 V
2114	5322 124 21711	100 µF	25 V
2115	4822 122 31759	22 nF	
2116	4822 122 31759	22 nF	
2117	4822 122 31759	22 nF	
2118	4822 122 31759	22 nF	
2119	4822 122 31759	22 nF	
2120	4822 122 31759	22 nF	
2121	4822 122 31759	22 nF	
2122	4822 122 31759	22 nF	
2123	4822 122 31759	22 nF	
2124	4822 122 31759	22 nF	

GEN LOCK MODULE G

(MOD LEVEL 3)

2006 A 3	2010 A 3	2018 B 7	2023 A 4	2026 B 4	3002 B 6	3056 A 4	6002 A 2	6005 B 3	6008 A 1	6013 A 3	6016 B 3	7017 B 4	7203 B 3	7206 A 4	7209 B 5
2007 A 3	2015 A 2	2020 B 1	2024 A 6	2043 B 5	3004 A 2	5001 B 3	6003 B 1	6006 B 3	6011 A 2	6014 B 3	7005 A 3	7201 A 2	7204 A 3	7207 A 5	
2008 A 1	2016 B 7	2022 B 5	2025 B 4	3001 B 7	3051 B 4	6001 B 1	6004 B 2	6007 A 2	6012 A 3	6015 B 4	7012 A 3	7202 B 1	7205 B 4	7208 B 5	



ADJUSTMENTS

Required
Test disc
Voltmeter

Adjustment conditions
Rotating disc

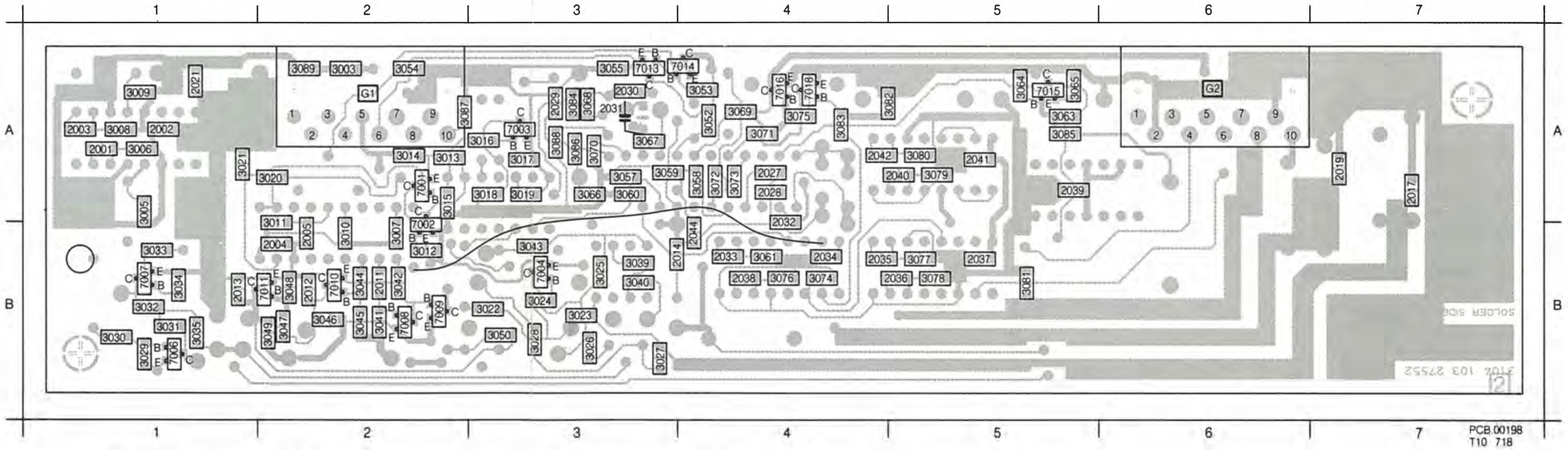
Adjustments

1) L5001 (VCO)
   - Measure the DC voltage on 4G2 and adjust L5001 until this voltage is 0V ± 2V.
     Note: In cold state of the set, adjust for + 2V.

Adjustment when item replaced

replaced	**adjust**
IC7205	L5001

2001 A 1	2013 B 1	2029 A 3	2036 B 5	2044 B 4	3010 B 2	3017 A 3	3024 B 3	3031 B 1	3041 B 2	3048 B 2	3057 A 3	3065 A 5	3072 A 4	3079 A 5	3086 A 3	7001 A 2	7011 B 2
2002 A 1	2014 B 4	2030 A 3	2037 B 5	3003 A 2	3011 B 2	3018 A 3	3025 B 3	3032 B 1	3042 B 2	3049 B 2	3058 A 4	3066 A 3	3073 A 4	3080 A 5	3087 A 3	7002 B 2	7014 A 4
2003 A 1	2017 A 7	2031 A 3	2038 B 4	3005 A 1	3012 B 2	3019 A 3	3026 B 3	3033 B 1	3043 B 3	3050 B 3	3059 A 3	3067 A 3	3074 B 4	3081 B 5	3088 A 3	7003 A 3	7015 A 5
2004 B 2	2019 A 7	2032 B 4	2039 A 5	3006 A 1	3013 A 2	3020 A 2	3027 B 3	3034 B 1	3044 B 2	3052 A 4	3060 A 3	3068 A 3	3075 A 4	3082 A 5	3089 A 2	7004 B 3	7016 A 4
2005 B 2	2021 A 1	2033 B 4	2040 A 5	3007 B 2	3014 A 2	3021 A 1	3028 B 3	3035 B 1	3045 B 2	3053 A 4	3061 B 4	3069 A 4	3076 B 4	3083 A 4	7008 B 2	7006 B 1	7018 A 4
2011 B 2	2027 A 4	2034 B 4	2041 A 5	3008 A 1	3015 A 2	3022 B 3	3029 B 1	3039 B 3	3046 B 2	3054 A 2	3063 A 5	3070 A 3	3077 B 5	3084 A 3	7009 B 2	7007 B 1	
2012 B 2	2028 A 4	2035 B 4	2042 A 4	3009 A 1	3016 A 3	3023 B 3	3030 B 1	3040 B 3	3047 B 2	3055 A 3	3064 A 5	3071 A 4	3078 B 5	3085 A 5	7013 A 3	7010 B 2	



PCB 00198
T10 718

LIST OF ELECTRICAL PARTS MODULE G

Coils

5001	4822 156 11004	26.5 μH

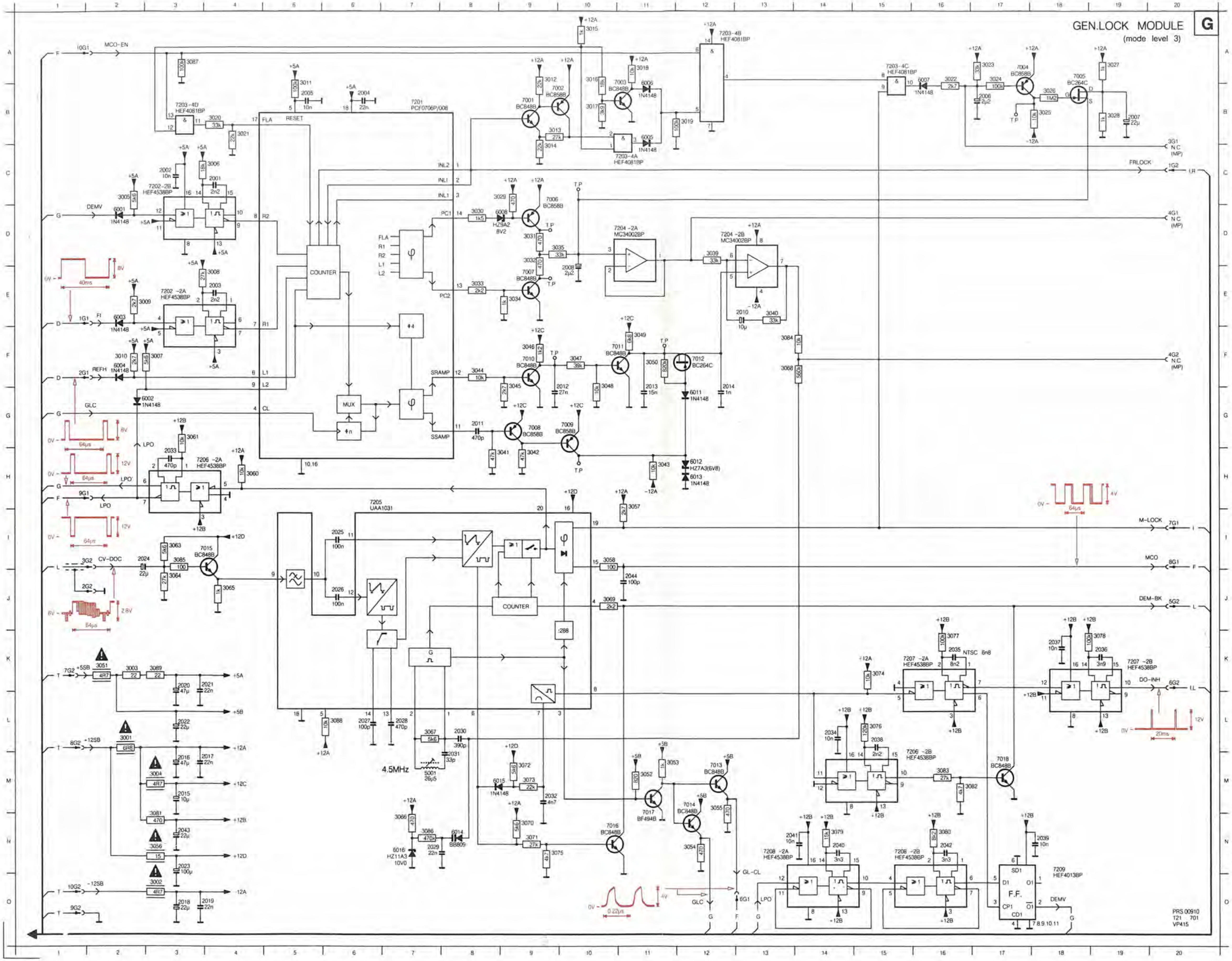
Fuse Resistors

3001	4822 111 30846	6.8 Ω
3002	5322 111 90376	4.7 Ω
3004	5322 111 90376	4.7 Ω
3051	5322 111 90376	4.7 Ω

NFR25 Resistors

3056	4822 111 30513	15 Ω

2001	4822 122 31644	2.2 nF		2024	5322 124 21643	22 μF	40 V
2002	4822 122 32442	10 nF		2025	4822 121 41608	100 nF	100 V
2003	4822 122 31644	2.2 nF		2026	4822 121 41608	100 nF	100 V
2004	4822 122 31759	22 nF		2027	4822 122 32974	100 pF	
2005	4822 122 32442	10 nF		2028	4822 122 32976	470 pF	
2006	4822 124 22029	2.2 μF	63 V	2029	4822 122 31759	22 nF	
2007	5322 124 21643	22 μF	40 V	2030	4822 122 31771	390 pF	
2008	4822 124 21255	2.2 μF	25 V	2031	5322 122 32104	33 pF	
2010	5322 124 21976	10 μF	25 V	2032	4822 122 31784	4.7 nF	
2011	4822 122 32976	470 pF		2033	4822 122 32976	470 pF	
2012	4822 122 32541	27 nF		2059	5322 124 14081	6.8 μF	25 V
2013	4822 122 31782	15 nF		2060	4822 122 31759	22 nF	
2014	5322 122 31647	1 nF		2061	4822 122 31965	220 pF	
2015	5322 124 21749	10 μF	63 V	2062	5322 124 21643	22 μF	40 V
2016	4822 124 22027	47 μF	25 V	2063	4822 122 31759	22 nF	
2017	4822 122 31759	22 nF		2064	4822 122 31759	22 nF	
2018	5322 124 21643	22 μF	40 V	2065	5322 124 21643	22 μF	40 V
2019	4822 122 31759	22 nF		2066	4822 122 31759	22 nF	
2020	4822 124 22027	47 μF	25 V	2067	4822 122 31774	56 pF	
2021	4822 122 31759	22 nF		2068	4822 122 31759	22 nF	
2022	5322 124 21643	22 μF	40 V	2069	4822 122 31072	47 pF	
2023	5322 124 21711	100 μF	25 V	2070	4822 124 22231	470 μF	



2001	C 4	6016	N 7
2002	C 3	7001	B 9
2003	E 4	7002	B10
2004	B 6	7003	A11
2005	B 5	7004	A17
2006	B17	7005	A18
2007	B19	7006	C 9
2008	E10	7007	E 9
2010	E13	7008	G 9
2011	G 8	7009	G10
2012	F10	7010	F 9
2013	F11	7011	F11
2014	F12	7012	F12
2015	M 3	7013	M12
2016	M 3	7014	M12
2017	M 4	7015	I 4
2018	O 3	7016	N10
2019	O 4	7017	M11
2020	K 3	7018	M17
2021	K 4	7201	B 7
2022	L 3	7202	E 3
2023	N 3	7202	C 3
2024	I 2	7203	B 3
2025	I 6	7203	C11
2026	J 6	7203	A12
2027	L 6	7203	A15
2028	L 7	7204	D11
2029	N 7	7204	D12
2030	L 8	7205	H 6
2031	M 8	7206	H 4
2032	M 9	7206	L16
2033	H 3	7207	K19
2034	L14	7207	K15
2035	K16	7208	N13
2036	K19	7208	N15
2037	K18	7209	N18
2038	L15		
2039	N18		
2040	N14		
2041	N14		
2042	N16		
2043	N 3		
2044	J11		
3001	L 2		
3002	O 3		
3003	K 2		
3004	M 3		
3005	C 2		
3006	C 4		
3007	F 3		
3008	E 4		
3009	E 3		
3010	F 2		
3011	A 5		
3012	A 9		
3013	B 9		
3014	C 9		
3015	A10		
3016	A10		
3017	B10		
3018	A11		
3019	B12		
3020	B 4		
3021	B 4		
3022	A16		
3023	A17		
3024	A17		
3025	B18		
3026	B18		
3027	A19		
3028	B19		
3029	C 9		
3030	D 8		
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3032	D 9		
3033	E 8		
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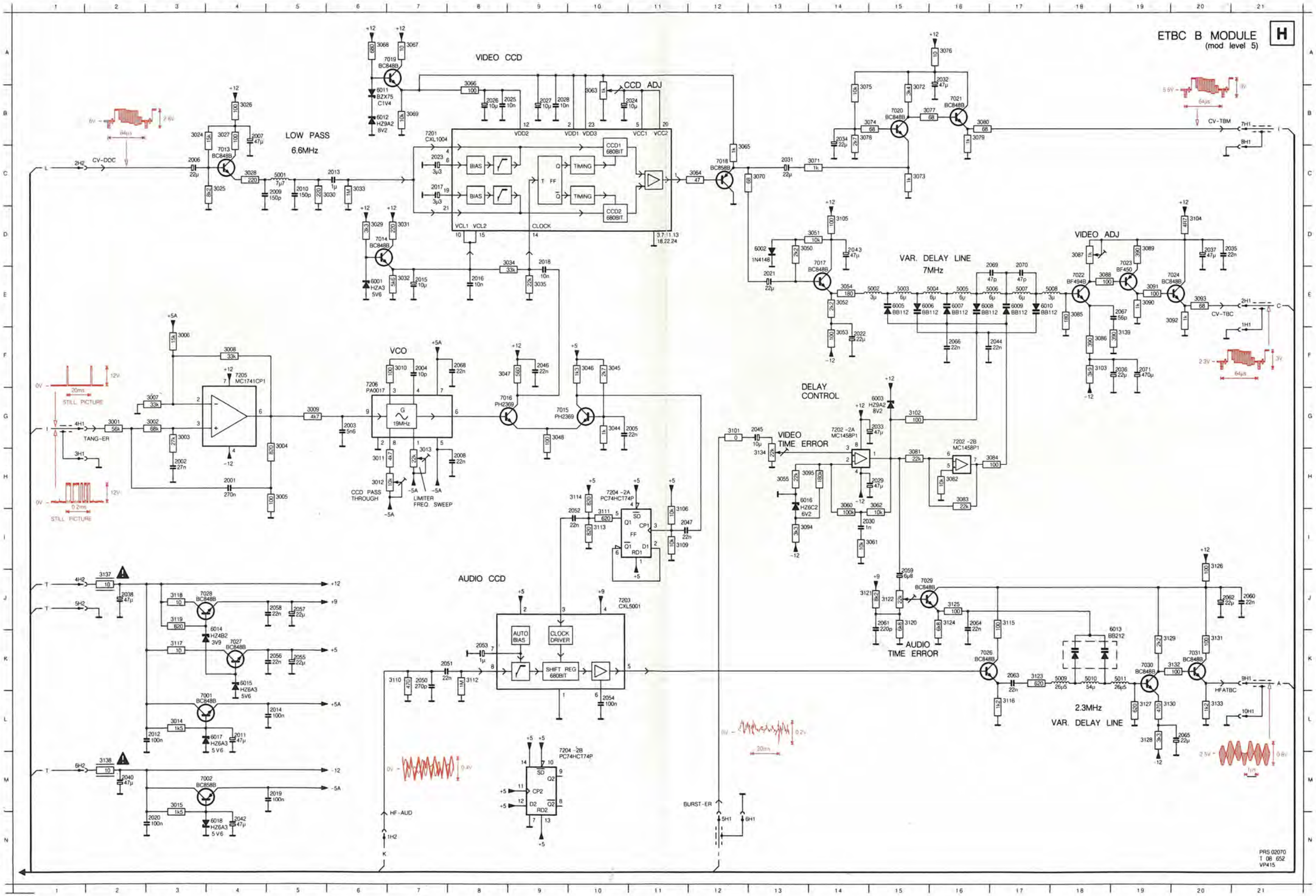
3035	D10		
3039	D12		
3040	E13		
3041	H 9		
3042	H 9		
3043	H11		
3044	F 8		
3045	F 9		
3046	F 9		
3047	F10		
3048	F10		
3049	F11		
3050	F11		
3051	K 2		
3052	M11		
3053	M11		
3054	N12		
3055	M12		
3056	N 3		
3057	H11		
3058	I 10		
3060	H 4		
3061	G 3		
3063	I 3		
3064	J 3		
3065	J 4		
3066	N 7		
3067	L 7		
3068	F13		
3069	J10		
3070	N 9		
3071	N 9		
3072	M 9		
3073	M 9		
3074	K15		
3075	N10		
3076	L15		
3077	K16		
3078	K19		
3079	N14		
3080	N16		
3081	M 3		
3082	M17		
3083	M16		
3084	F13		
3085	I 3		
3086	N 7		
3087	A 3		
3088	L 6		
3089	K 3		
5001	M 7		
6001	D 2		
6002	G 3		
6003	E 2		
6004	F 2		
6005	B11		
6006	A11		
6007	A16		
6008	D 9		
6011	G12		
6012	H12		
6013	H12		
6014	N 8		
6015	M 8		

CS 6 873

2001	H 4	2009	C 5	2017	C 7	2025	B 9	2033	G15	2043	D14	2053	K 8	2061	J15	2069	D17	3006	F 3	3014	L 3	3030	C 6	3046	F10	3055	H13	3067	A 7	3075	B14	3083	H16	3091	E19	3104	D20	3114	H10	3122	J15	3130	L20	5001	C 5	5009	K18	6007	E16	6015	K 4	7015	G 9	7023	D19	7201	B 7
2002	H 3	2010	C 5	2018	D 9	2026	B 8	2034	B14	2044	F17	2054	L10	2062	J20	2070	D17	3007	G 3	3015	M 3	3031	D 7	3047	F 8	3060	H14	3068	A 6	3076	A16	3084	H17	3092	E20	3105	D14	3115	J17	3123	K17	3131	K20	5002	E15	5010	K18	6008	E17	6016	H14	7016	G 8	7024	E20	7202	G14
2003	G 6	2011	L 4	2019	M 5	2027	B 9	2035	D21	2045	G13	2055	K 5	2063	K17	2071	F19	3008	F 4	3024	B 3	3032	E 7	3048	G 9	3061	I 15	3069	B 7	3077	B16	3085	E18	3093	E20	3106	I 11	3116	L17	3124	J16	3132	K20	5003	E15	5011	K19	6009	E17	6017	L 4	7017	D14	7026	K16	7202	G16
2004	F 7	2012	L 3	2020	N 3	2028	B 9	2036	F19	2046	F 9	2056	K 5	2064	J16	3001	G 2	3009	G 5	3025	C 4	3033	C 6	3050	D14	3062	H15	3070	C13	3078	B14	3086	F18	3094	I 14	3109	I 11	3117	K 3	3125	J16	3133	L20	5004	E16	6001	E 6	6010	E17	6018	N 4	7018	C12	7027	K 4	7203	J10
2005	G11	2013	C 6	2021	E13	2029	H15	2037	D20	2047	I 11	2057	J 5	2065	L20	3002	G 3	3010	F 7	3026	B 4	3034	D 9	3051	D14	3063	B10	3071	C14	3079	B16	3087	D18	3095	H14	3110	K 7	3118	J 3	3126	I 20	3134	H13	5005	E16	6002	D13	6011	B 6	7001	L 4	7019	A 7	7028	J 4	7204	L 9
2006	C 3	2014	L 5	2022	F14	2030	I 15	2038	J 2	2050	K 7	2058	J 5	2066	F16	3003	G 3	3011	H 6	3027	B 4	3035	E 9	3052	E14	3064	C12	3072	B15	3080	B16	3088	E18	3101	G12	3111	I 10	3119	J 3	3127	L19	3137	J 2	5006	E17	6003	G15	6012	B 6	7002	M 4	7020	B15	7029	J15	7204	H10
2007	B 4	2015	E 7	2023	C 7	2031	C13	2040	M 2	2051	K 7	2059	J15	2067	E19	3004	G 5	3012	H 6	3028	C 4	3044	G10	3053	F14	3065	C12	3073	C15	3081	H15	3089	D19	3102	G15	3112	K 8	3120	J15	3128	L19	3138	M 2	5007	E17	6005	E15	6013	J19	7013	C 4	7021	B16	7030	K19	7205	F 4
2008	H 8	2016	E 8	2024	B11	2032	A16	2042	N 4	2052	I 10	2060	J21	2068	F 8	3005	H 5	3013	H 7	3029	D 6	3045	F10	3054	E14	3066	A 8	3074	B15	3082	H16	3090	E19	3103	F18	3113	I 10	3121	J14	3129	K20	3139	F19	5008	E18	6006	E16	6014	J 4	7014	D 6	7022	E18	7031	K20	7206	F 6



ETBC-B MODULE **H**

(MOD. LEVEL 5)

ADJUSTMENTS

Required
Test disc
Scope
DC supply

Adjustment conditions
Load test disc.
Still picture, colour bar (picture no. 6200).

Adjustments

1) **R3012, R3013** (CCD pass-through, limiter freq. sweep)
   - Using the scope, measure signal CV-DOC on 2H2 (A channel) and CV-TBC on 2H1 (B channel).
   - Short-circuit C2003 (9-IC7206 to ground).
   - Display the first lines of the video signal on the scope by means of the DTB.
   - Adjust R3012 for a delay of 70 µsec ± 1 µsec between the two signals.
   - Remove the short-circuit of C2003.
   - Connect with the DC supply a variable voltage to junction R3001, R3002, C2001 (TANG-ER).
   - Measure the delay of the CV-DOC and CV-TBC signals as a function of the DC voltage presented:
     0V : 46 µsec ± 1.5 µsec
     +3V : 70 µsec ± 1 µsec
     +5V : 91 µsec ± 1.5 µsec
     Correct deviations by adjusting R3013.

2) **R3063** (CCD adjust)
   - Search for pict. no. 470 (white).
   - Measure the CV-TBM signal on p.1-IC7201 with the scope.
   - Adjust R3063 for a black level amplitude of 3,2Vpp.
   - The CV-TBM signal on 7H1 is shown in fig. H1.

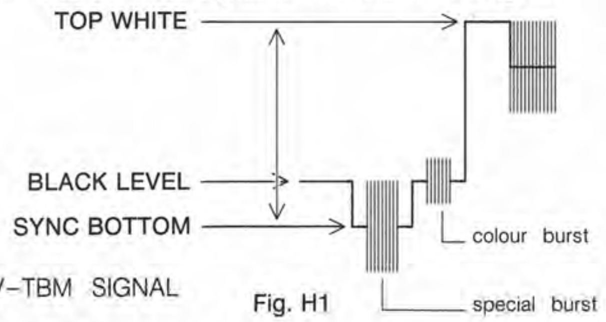


Fig. H1

3) **R3087 (Video adjust)**
   - Measure the CVBS OUT-signal on BNC3 (rear) with the scope (75 Ω terminated).
   - Press switch SK2 on analog I/O module U (pos. NOT ENCODED).
   - Adjust R3087 for a CVBS amplitude (top white-sync bottom) of 1 Vpp.
   - Switch SK2 back into the earlier position.

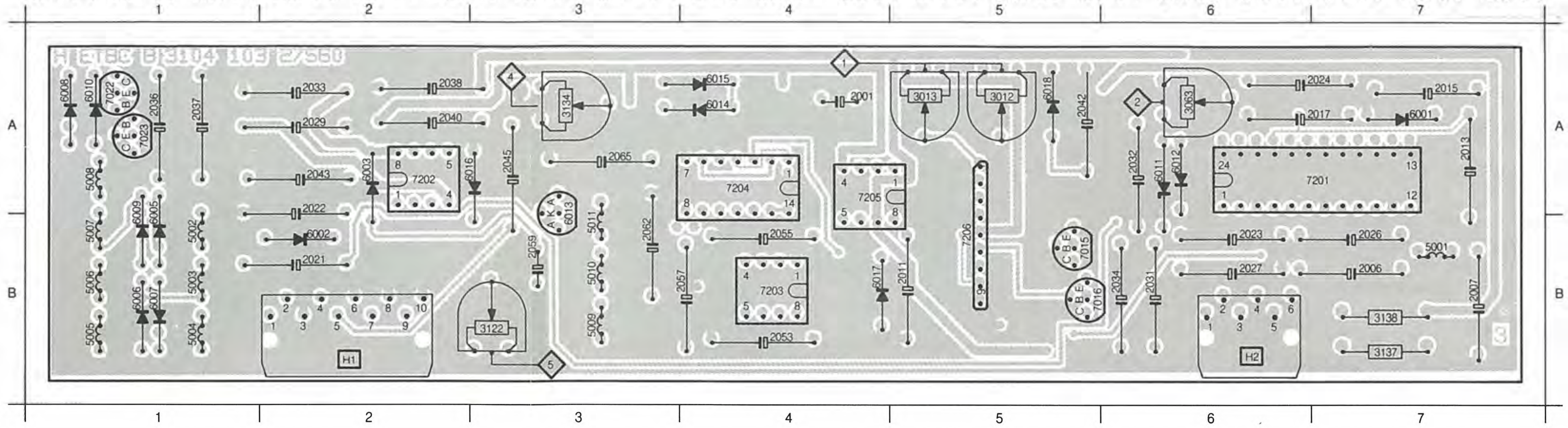
4) **R3134** (video time errors)
   - Search picture no. 1000 (blue picture) and adjust R3134 for minimum dark bars.
   - Search picture no 1800 (yellow picture) and adjust R3134 for minimum red stripes.
   - Repeat these two adjustments if necessary.

5) **R3122** (audio time errors)
   - Switch the player into the normal play mode with sound modulation.
   - Measure the AC signal on E-TS7029 and adjust R3122 for minimum AC.

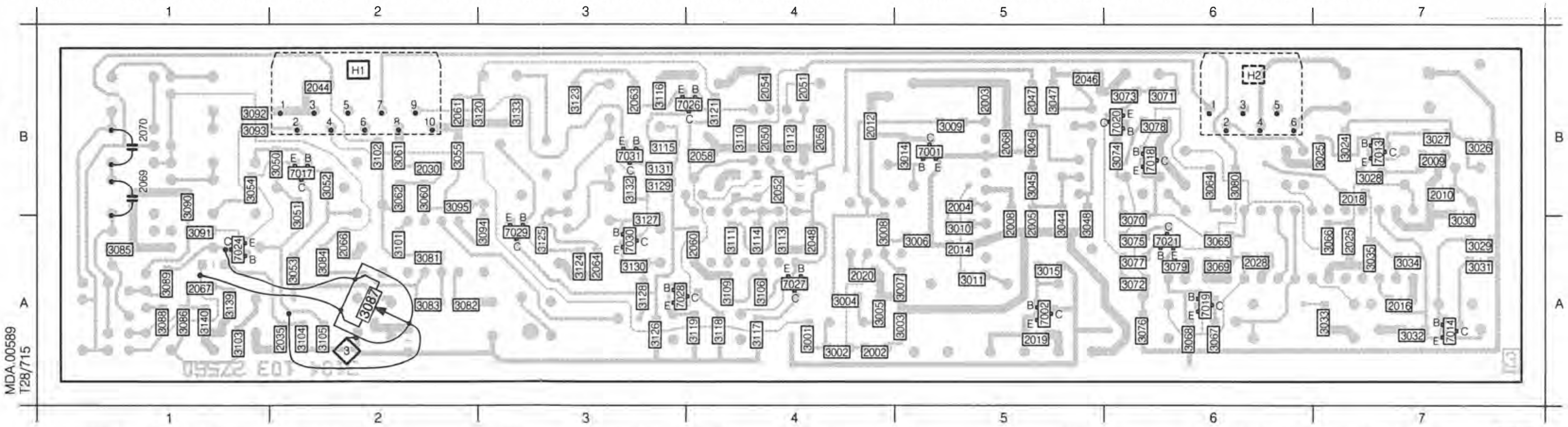
Adjustment when item replaced

replaced	adjust
IC7201	R3063, R3087
IC7206	R3012, R3013

2001 A 4	2013 A 7	2022 A 2	2027 B 6	2033 A 2	2038 A 2	2045 A 3	2059 B 3	3013 A 5	3137 B 7	5003 B 1	5007 B 1	5011 B 3	6005 A 1	6009 A 1	6013 A 3	6017 B 4	7022 A 1	7203 B 4
2006 B 7	2015 A 7	2023 B 6	2029 A 2	2034 B 6	2040 A 2	2053 B 4	2062 B 3	3063 A 6	3138 B 7	5004 B 1	5008 A 1	6001 A 7	6006 B 1	6010 A 1	6014 A 4	6018 A 5	7023 A 1	7204 A 4
2007 B 7	2017 A 7	2024 A 7	2031 B 6	2036 A 1	2042 A 5	2055 B 4	2065 A 3	3122 B 3	5001 B 7	5005 B 1	5009 B 3	6002 B 2	6007 B 1	6011 A 6	6015 A 4	7015 B 5	7201 A 7	7205 A 4
2011 B 5	2021 B 2	2026 B 7	2032 A 6	2037 A 1	2043 A 2	2057 B 4	3012 A 5	3134 A 3	5002 B 1	5006 B 1	5010 B 3	6003 A 2	6008 A 1	6012 A 6	6016 A 2	7016 B 5	7202 A 2	7206 B 5



2002 A 4	2016 A 7	2046 B 5	2060 A 4	3001 A 4	3010 A 5	3029 A 7	3046 B 5	3060 A 2	3070 A 6	3079 A 6	3087 A 2	3101 A 2	3112 B 4	3121 B 4	3131 B 3	7017 B 2	7029 A 3
2003 B 5	2018 B 7	2047 B 5	2061 B 2	3002 A 4	3011 A 5	3030 A 7	3047 B 5	3061 B 2	3071 B 6	3080 B 6	3088 A 1	3102 B 2	3113 A 4	3123 B 3	3132 A 3	7018 B 6	7030 A 3
2004 B 5	2019 A 5	2048 A 4	2063 B 3	3003 A 5	3014 B 5	3031 A 7	3048 A 5	3062 A 2	3072 A 6	3081 A 2	3089 A 1	3103 A 1	3114 A 4	3124 A 3	3133 B 3	7019 A 6	7031 B 3
2005 A 5	2020 A 4	2050 B 4	2064 A 3	3004 A 4	3015 A 5	3032 A 7	3050 B 2	3064 B 6	3073 B 6	3082 A 2	3090 A 1	3104 A 2	3115 B 3	3125 A 3	3139 A 1	7020 B 6	
2008 A 5	2025 A 7	2051 B 4	2066 A 2	3005 A 4	3024 B 7	3033 A 7	3051 A 2	3065 A 6	3074 B 6	3083 A 2	3091 A 1	3105 A 2	3116 B 3	3126 A 3	3140 A 1	7021 A 6	
2009 B 7	2028 A 6	2052 A 4	2067 A 1	3006 A 5	3025 B 7	3034 A 7	3052 B 2	3066 A 7	3075 A 6	3084 A 2	3092 B 1	3106 A 4	3117 A 4	3127 A 3	7001 B 5	7024 A 1	
2010 B 7	2030 B 2	2054 B 4	2068 B 5	3007 A 5	3026 B 7	3035 A 7	3053 A 2	3067 A 6	3076 A 6	3085 A 1	3093 B 1	3109 A 4	3118 A 4	3128 A 3	7002 A 5	7026 B 4	
2012 B 4	2035 A 2	2056 B 4	2069 B 1	3008 A 4	3027 B 7	3044 A 5	3054 A 1	3068 A 6	3077 A 6	3086 A 1	3094 A 3	3110 B 4	3119 A 4	3129 B 3	7013 B 7	7027 A 4	
2014 A 5	2044 B 2	2058 B 4	2070 B 1	3009 B 5	3028 B 7	3045 B 5	3055 B 2	3069 A 6	3078 B 6		3095 B 2	3111 A 4	3120 B 3	3130 A 3	7014 A 7	7028 A 3	



MDA 00589
T28/715

PCB 01004
T03/718

LIST OF ELECTRICAL PARTS MODULE H

Coils

5001	4822 156 11002	7.7 µH
5002	4822 156 10998	3 µH
5003	4822 156 11001	6 µH
5004	4822 156 11001	6 µH
5005	4822 156 11001	6 µH
5006	4822 156 11001	6 µH
5007	4822 156 11001	6 µH
5008	4822 156 10998	3 µH
5009	4822 156 11004	26.5 µH
5010	4822 156 11006	54 µH
5011	4822 156 11004	26.5 µH

Potentiometers

3012	5322 101 10627	10 kΩ
3013	5322 101 10628	22 kΩ
3063	4822 100 20151	1 kΩ
3087	4822 100 10254	1 kΩ
3122	5322 101 10628	22 kΩ
3134	5322 101 10628	22 kΩ

Fuse Resistors

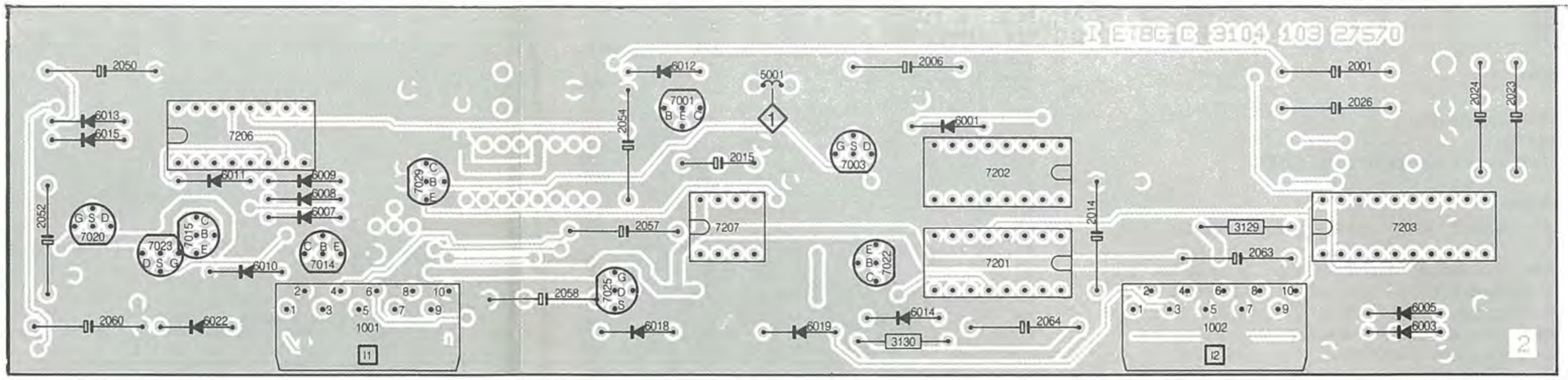
3137	4822 111 10165	10Ω
3138	4822 111 10165	10Ω

2001	4822 121 41874	270 nF	63 V
2002	4822 122 32541	27 nF	
2003	4822 122 31916	5.6 nF	
2004	4822 122 31971	10 pF	
2005	4822 122 31759	22 nF	
2006	5322 124 21643	22 µF	40 V
2007	4822 124 22027	47 µF	25 V
2008	4822 122 31759	22 nF	
2009	4822 122 31767	150 pF	
2010	4822 122 31767	150 pF	
2011	4822 124 22027	47 µF	25 V
2012	5322 122 32839	100 nF	
2013	4822 121 41719	1 µF	10% 100 V
2014	5322 122 32839	100 nF	
2015	5322 124 21749	10 µF	63 V
2016	4822 122 32442	10 nF	
2017	4822 124 22188	3.3 µF	63 V
2018	4822 122 32442	10 nF	
2019	5322 122 32839	100 nF	
2020	5322 122 32839	100 nF	
2021	5322 124 21643	22 µF	40 V
2022	5322 124 21643	22 µF	40 V
2023	4822 124 22188	3.3 µF	63 V
2024	5322 124 21749	10 µF	63 V
2025	4822 122 32442	10 nF	
2026	5322 124 21749	10 µF	63 V
2027	5322 124 21749	10 µF	63 V
2028	4822 122 32442	10 nF	
2029	4822 124 22027	47 µF	25 V
2030	5322 122 31647	1 nF	
2031	5322 124 21643	22 µF	40 V
2032	4822 124 22027	47 µF	25 V
2033	4822 124 22027	47 µF	25 V
2034	5322 124 21643	22 µF	40 V
2035	4822 122 31759	22 nF	
2036	5322 124 21643	22 µF	40 V
2037	4822 124 22027	47 µF	25 V
2038	4822 124 22027	47 µF	25 V
2040	4822 124 22027	47 µF	25 V
2042	4822 124 22027	47 µF	25 V
2043	4822 124 22027	47 µF	25 V
2044	4822 122 31759	22 nF	
2045	5322 124 21749	10 µF	63 V
2046	4822 122 31759	22 nF	
2047	4822 122 31759	22 nF	
2050	4822 122 32142	270 pF	
2051	4822 122 31759	22 nF	
2052	4822 122 31759	22 nF	
2053	4822 124 22028	1 µF	63 V
2054	5322 122 32839	100 nF	
2055	5322 124 21643	22 µF	40 V
2056	4822 122 31759	22 nF	
2057	5322 124 21643	22 µF	40 V
2058	4822 122 31759	22 nF	

ETBC C MODULE I

(MOD LEVEL 6)

1001 B 2	2006 A 5	2023 A 7	2050 A 1	2057 B 3	2063 B 6	3130 B 5	6003 B 7	6008 A 2	6011 A 2	6014 B 5	6019 B 4	7003 •A 4	7020 B 1	7025 B 3	7202 A 5	7207 B 4
1002 B 6	2014 B 5	2024 A 7	2052 B 1	2058 B 3	2064 B 5	5001 A 4	6005 B 7	6009 A 2	6012 A 4	6015 A 1	6022 B 1	7014 B 2	7022 B 4	7029 A 2	7203 B 7	
2001 A 7	2015 A 4	2026 A 7	2054 A 3	2060 B 1	3129 B 6	6001 A 5	6007 B 2	6010 B 2	6013 A 1	6018 B 3	7001 A 4	7015 B 1	7023 B 1	7201 B 5	7206 A 2	



ADJUSTMENTS

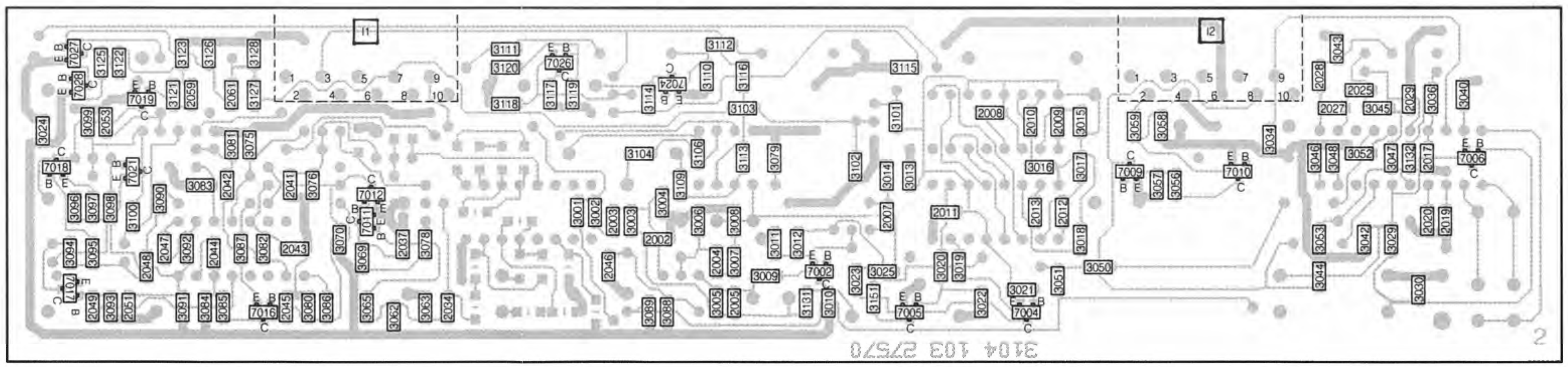
Required
Test disc
Scope

Adjustment conditions
Load test disc.
Still picture, colour bar (picture no. 6200).

Adjustment

1) **L5001** (Special burst separator)
   - Measure the signal on B–TS7029 with the scope (line– frequent).
   - Adjust L5001 for maximum amplitude of the special burst signal.

2002 A 3	2011 A 5	2028 B 6	2045 A 2	2061 B 2	3008 A 4	3016 B 5	3024 B 1	3043 B 6	3052 B 7	3065 A 2	3081 B 2	3089 A 3	3097 A 1	3106 B 4	3116 B 4	3125 B 1	7004 A 5	7017 A. 1
2003 A 3	2012 A 5	2029 B 7	2046 A 3	3001 A 3	3009 A 4	3017 A 5	3025 A 4	3044 A 6	3053 A 6	3069 A 2	3082 A 2	3090 A 1	3098 A 1	3109 A 4	3117 B 3	3126 B 1	7005 A 5	7018 B 1
2004 A 4	2013 A 5	2034 A 2	2047 A 1	3002 A 3	3010 A 4	3018 A 5	3029 A 7	3045 B 7	3056 A 6	3070 A 2	3083 A 1	3091 A 1	3099 B 1	3110 B 4	3118 B 3	3127 B 2	7006 B 7	7019 B 1
2005 A 4	2017 A 7	2037 A 2	2048 A 1	3003 A 3	3011 A 4	3019 A 5	3030 A 7	3046 A 6	3057 A 6	3075 B 2	3084 A 1	3092 A 1	3100 A 1	3111 B 3	3119 B 3	3128 B 2	7009 B 6	7021 A 1
2007 A 4	2019 A 7	2041 A 2	2049 A 1	3004 A 3	3012 A 4	3020 A 5	3034 B 6	3047 A 7	3058 B 6	3076 A 2	3085 A 1	3093 A 1	3101 B 5	3112 B 4	3120 B 3	3131 A 4	7010 B 6	7024 B 4
2008 B 5	2020 A 7	2042 A 1	2051 A 1	3005 A 4	3013 A 5	3021 A 5	3036 B 7	3048 A 6	3059 B 6	3078 A 2	3086 A 2	3094 A 1	3102 A 4	3113 A 4	3121 B 1	3132 A 7	7011 A 2	7026 B 3
2009 B 5	2025 B 7	2043 A 2	2053 B 1	3006 A 4	3014 A 4	3022 A 5	3040 B 7	3050 A 5	3062 A 2	3079 A 4	3087 A 2	3095 A 1	3103 B 4	3114 B 3	3122 B 1	3151 A 4	7012 A 2	7027 B 1
2010 B 5	2027 B 6	2044 A 1	2059 B 1	3007 A 4	3015 B 5	3023 A 4	3042 A 7	3051 A 5	3063 A 2	3080 A 2	3088 A 3	3096 A 1	3104 B 3	3115 B 5	3123 B 1	7002 A 4	7016 A 2	7028 B 1



PCB.01005
T10 718

LIST OF ELECTRICAL PARTS MODULE I

Coils

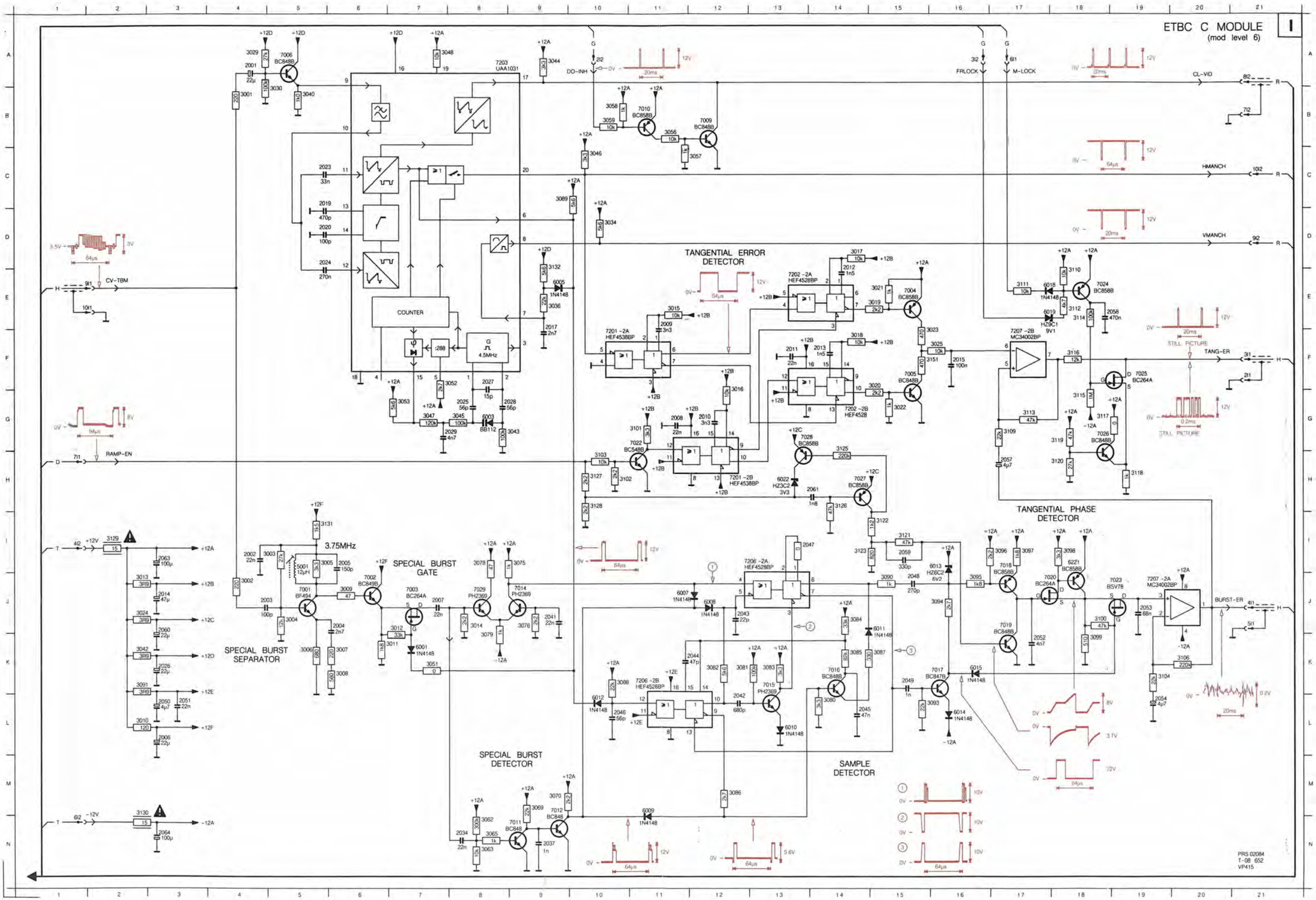
5001	4822 156 11003	12 µH

NFR25 Resistors

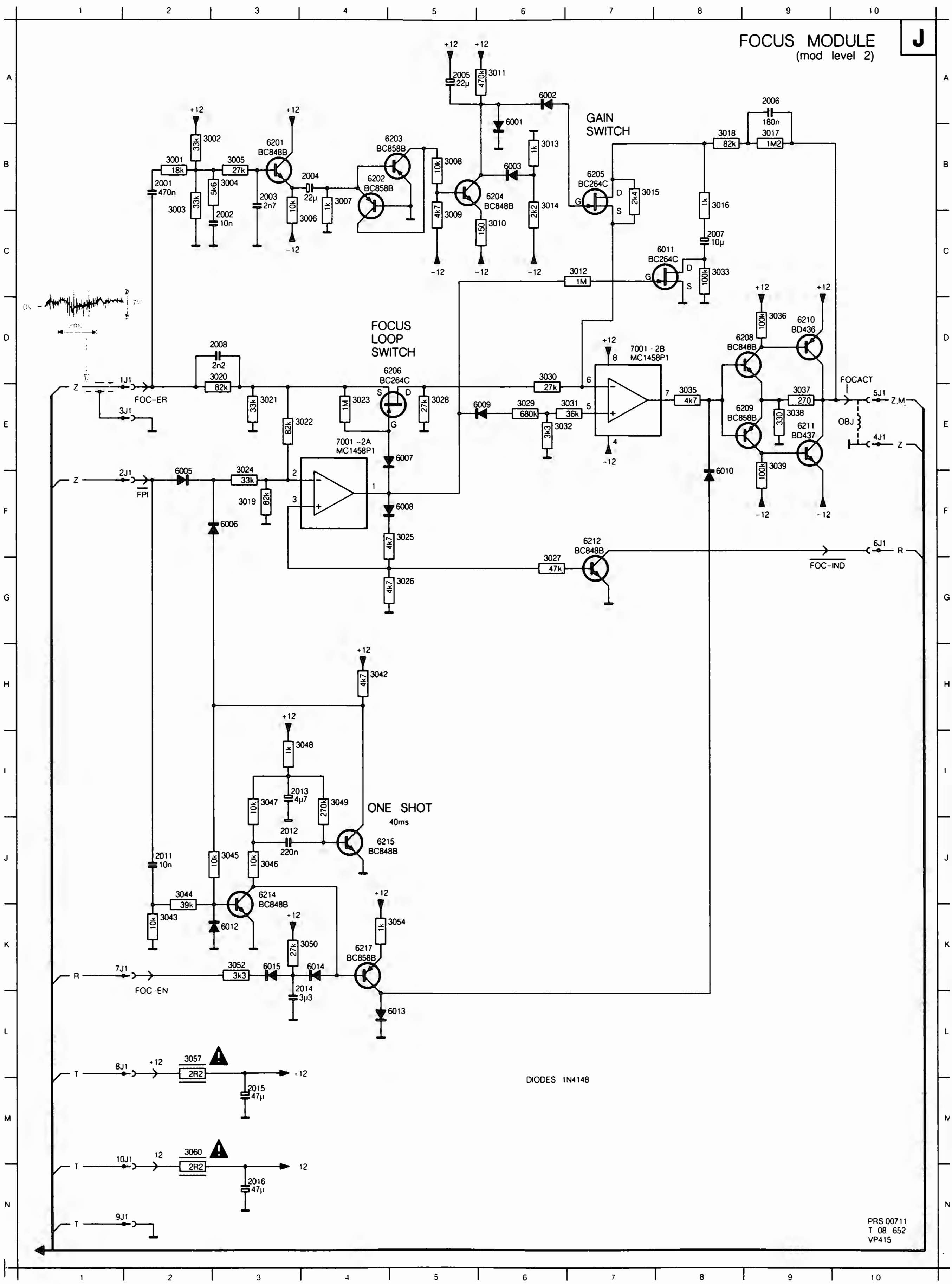
3129	4822 111 30513	15 Ω
3130	4822 111 30513	15 Ω

2001	5322 124 21643	22 µF	40 V
2002	4822 122 31759	22 nF	
2003	4822 122 32974	100 pF	
2004	4822 122 31783	2.7 nF	
2005	4822 122 31767	150 pF	
2006	5322 124 21643	22 µF	40 V
2007	4822 122 31759	22 nF	
2008	4822 122 31759	22 nF	
2009	4822 122 31969	3.3 nF	
2010	4822 122 31969	3.3 nF	
2011	4822 122 31759	22 nF	
2012	4822 122 31781	1.5 nF	
2013	4822 122 31781	1.5 nF	
2014	4822 124 22027	47 µF	25 V
2015	4822 121 41608	100 nF	100 V
2017	4822 122 31783	2.7 nF	
2019	4822 122 32976	470 pF	
2020	4822 122 32974	100 pF	
2023	4822 121 41545	33 nF	250 V
2024	4822 121 41874	270 nF	63 V
2025	4822 122 31774	56 pF	
2026	5322 124 21643	22 µF	40 V
2027	4822 122 32504	15 pF	
2028	4822 122 31774	56 pF	
2029	4822 122 31784	4.7 nF	
2034	4822 122 31759	22 nF	
2037	5322 122 31647	1 nF	
2041	4822 122 31759	22 nF	
2042	4822 122 31775	680 pF	
2043	4822 122 32482	22 pF	
2044	4822 122 31772	47 pF	
2045	4822 122 32542	47 nF	
2046	4822 122 31774	56 pF	
2048	4822 122 32142	270 pF	
2049	5322 122 31647	1 nF	
2050	4822 124 22031	4.7 µF	63 V
2051	4822 122 31759	22 nF	
2052	4822 121 51051	4.7 nF	160 V
2053	4822 122 32891	68 nF	
2054	4822 124 22031	4.7 µF	63 V
2057	4822 124 22031	4.7 µF	63 V
2058	4822 121 41757	470 nF10%	63 V
2059	4822 121 42915	330 pF	
2060	5322 124 21643	22 µF	40 V
2061	4822 122 32153	1.8 nF	
2063	5322 124 21711	100 µF	25 V
2064	5322 124 21711	100 µF	25 V

2001 A 4	2008 G11	2015 F16	2026 K 3	2042 L12	2049 K15	2058 E19	3002 J 4	3009 J 5	3016 F12	3023 F16	3040 B 5	3048 A 8	3059 B10	3076 J 9	3084 J14	3091 K 2	3099 K18	3109 G17	3116 F18	3123 I14	3131 I 6	6007 J11	6014 L16	7002 J 6	7011 N 9	7020 J17	7028 G13	7206 K11
2002 I 4	2009 E11	2017 E 9	2027 F 8	2043 J12	2050 L 3	2059 I15	3003 I 5	3010 L 2	3017 D14	3024 J 2	3042 K 2	3051 K 7	3062 N 8	3078 I 8	3085 K14	3093 L16	3100 J18	3110 E18	3117 G18	3125 G14	3132 D 9	6008 J12	6015 K16	7003 J 7	7012 M 9	7022 G11	7029 J 8	7206 I13
2003 J 4	2010 G12	2019 C 5	2028 G 9	2044 K12	2051 L 3	2060 J 3	3004 J 5	3011 K 7	3018 F14	3025 F16	3043 G 9	3052 F 8	3063 N 8	3079 K 8	3086 M12	3094 J16	3101 G11	3111 E17	3118 H19	3126 H14	3151 F16	6009 M11	6018 E17	7004 E15	7015 K13	7023 J19	7201 H12	7207 J19
2004 J 6	2011 F13	2020 D 5	2029 G 8	2045 L14	2052 K17	2061 H14	3005 I 6	3012 J 7	3019 E15	3029 A 4	3044 A 9	3053 G 7	3065 N 8	3080 L14	3087 K15	3095 J16	3102 H10	3112 E16	3119 G18	3127 H10	5001 I 5	6010 L13	6019 E17	7005 F15	7016 K14	7024 E18	7201 F10	7207 F17
2005 I 6	2012 D14	2023 C 5	2034 N 8	2046 L10	2053 J19	2063 I 3	3006 K 5	3013 J 2	3020 F15	3030 B 5	3045 G 8	3056 B11	3069 M 9	3081 K12	3088 K10	3096 I17	3103 H10	3113 G17	3120 H18	3128 H10	6001 K 7	6011 J15	6022 H13	7006 A 5	7017 K16	7025 F19	7202 G14	
2006 L 3	2013 F14	2024 D 5	2037 N 9	2047 I14	2054 L19	2064 N 3	3007 K 6	3014 J 8	3021 E15	3034 D10	3046 C10	3057 C12	3070 M 9	3082 K12	3089 C 9	3097 I17	3104 K19	3114 E18	3121 I15	3129 I 2	6003 G 8	6012 L10	6221 I18	7009 B12	7018 I17	7026 G18	7202 E13	
2007 J 7	2014 J 3	2025 G 8	2041 J 9	2048 J15	2057 H17	3001 B 4	3008 K 6	3015 E11	3022 G15	3036 E 9	3047 G 7	3058 B10	3075 I 9	3083 K13	3090 J15	3098 I18	3106 K20	3115 G16	3122 I15	3130 M 2	6005 E 9	6013 I16	7001 J 5	7010 B11	7019 J17	7027 H14	7203 A 8	



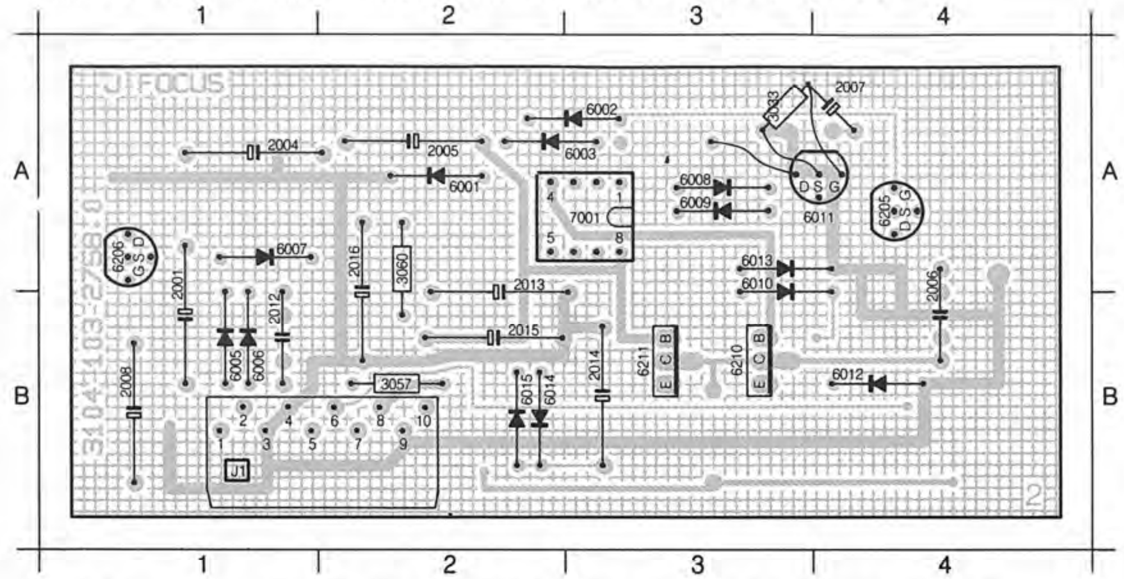
2001	B 2	2011	J 2	3003	B 2	3011	A 6	3019	F 3	3027	G 6	3036	D 9	3046	J 3	3060	M 2	6009	E 6	6202	B 4	6211	E 9
2002	C 3	2012	J 3	3004	B 3	3012	D 6	3020	D 3	3028	E 5	3037	E 9	3047	I 3	6001	A 6	6010	F 8	6203	B 5	6212	F 7
2003	B 3	2013	I 4	3005	B 3	3013	B 6	3021	E 3	3029	E 6	3038	E 9	3048	I 4	6002	A 6	6011	C 8	6204	B 6	6214	J 3
2004	B 4	2014	K 4	3006	C 4	3014	B 6	3022	E 4	3030	D 6	3039	E 9	3049	I 4	6003	B 6	6012	K 3	6205	B 7	6215	J 4
2005	A 5	2015	M 3	3007	B 4	3015	B 8	3023	E 4	3031	E 7	3042	H 4	3050	K 4	6005	F 2	6013	L 5	6206	D 5	6217	K 4
2006	A 9	2016	N 3	3008	B 5	3016	B 8	3024	E 3	3032	E 7	3043	K 2	3052	K 3	6006	F 3	6014	K 4	6208	D 9	7001	D 7
2007	B 8	3001	B 2	3009	C 5	3017	B 9	3025	F 5	3033	C 8	3044	J 2	3054	K 5	6007	E 5	6015	K 3	6209	E 9	7001	E 4
2008	D 3	3002	B 3	3010	C 6	3018	B 8	3026	G 5	3035	E 8	3045	J 3	3057	L 2	6008	F 5	6201	B 3	6210	D 9		



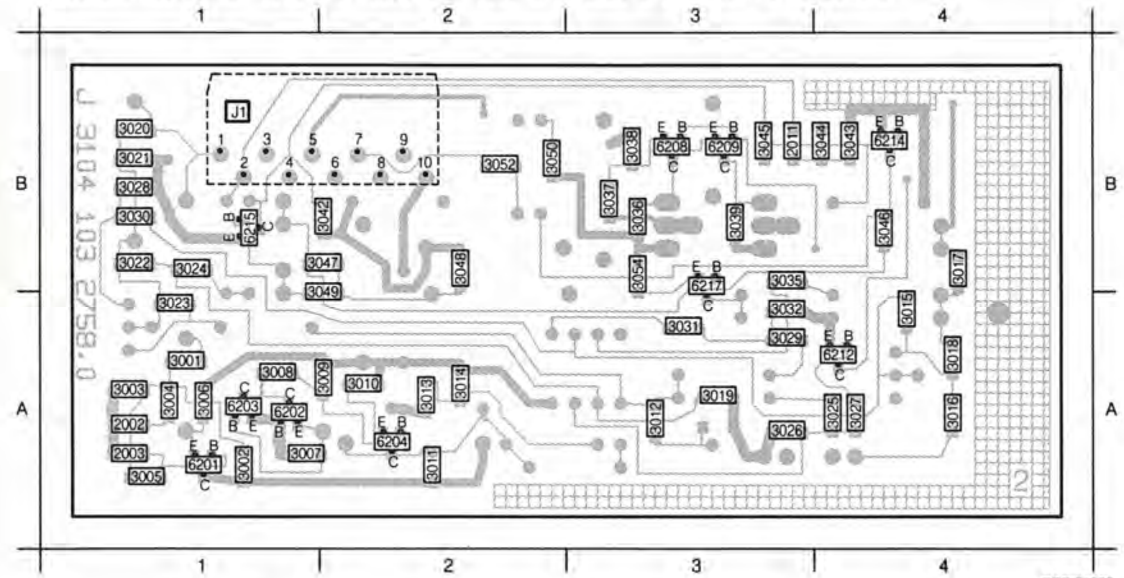
FOCUS MODULE J

(MOD. LEVEL 2)

2001 A 1	2007 A 4	2014 B 3	3057 B 2	6003 A 3	6008 A 3	6012 B 4	6205 A 4	7001 A 3
2004 A 1	2008 B 1	2015 B 2	3060 A 2	6005 B 1	6009 A 3	6013 A 3	6206 A 1	
2005 A 2	2012 B 1	2016 A 2	6001 A 2	6006 B 1	6010 A 3	6014 B 2	6210 B 3	
2006 A 4	2013 A 2	3033 A 3	6002 A 3	6007 A 1	6011 A 4	6015 B 2	6211 B 3	



2002 A 1	3005 A 1	3012 A 3	3019 A 3	3026 A 3	3035 B 3	3044 B 4	3052 B 2	6209 B 3
2003 A 1	3006 A 1	3013 A 2	3020 B 1	3027 A 4	3036 B 3	3045 B 3	3054 A 3	6212 A 4
2011 B 3	3007 A 1	3014 A 2	3021 B 1	3028 B 1	3037 B 3	3046 B 4	6201 A 1	6214 B 4
3001 A 1	3008 A 1	3015 A 4	3022 B 1	3029 A 3	3038 B 3	3047 B 2	6202 A 1	6215 B 1
3002 A 1	3009 A 2	3016 A 4	3023 A 1	3030 B 1	3039 B 3	3048 A 2	6203 A 1	6217 A 3
3003 A 1	3010 A 2	3017 A 4	3024 B 1	3031 A 3	3042 B 2	3049 A 2	6204 A 2	
3004 A 1	3011 A 2	3018 A 4	3025 A 4	3032 A 3	3043 B 4	3050 B 2	6208 B 3	



PCB 01006
T03/715

LIST OF ELECTRICAL PARTS MODULE J

NFR25 Resistors

3057	4822 111 30492	2.2 Ω
3060	4822 111 30492	2.2 Ω

2001	4822 122 33011	470 nF	16 V
2002	4822 122 32442	10 nF	
2003	4822 122 31783	2.7 nF	
2004	5322 124 21643	22 μF	40 V
2005	5322 124 21643	22 μF	40 V
2006	4822 121 42527	180 nF	63 V
2007	4822 124 21314	10 μF	10 V
2008	4822 121 50841	2.2 nF	160 V
2011	4822 122 32442	10 nF	
2012	4822 121 41876	220 nF	20% 63 V
2013	4822 124 22031	4.7 μF	63 V
2014	4822 124 22188	3.3 μF	63 V
2015	4822 124 22027	47 μF	25 V
2016	4822 124 22027	47 μF	25 V

HF PROC MODULE K

(MOD LEVEL 0)

ADJUSTMENTS

Required
Test disc
Scope
HF generator (100 kHz – 10 MHz)

Adjustment conditions
Load test disc
Still picture, picture no. 6200

Adjustments

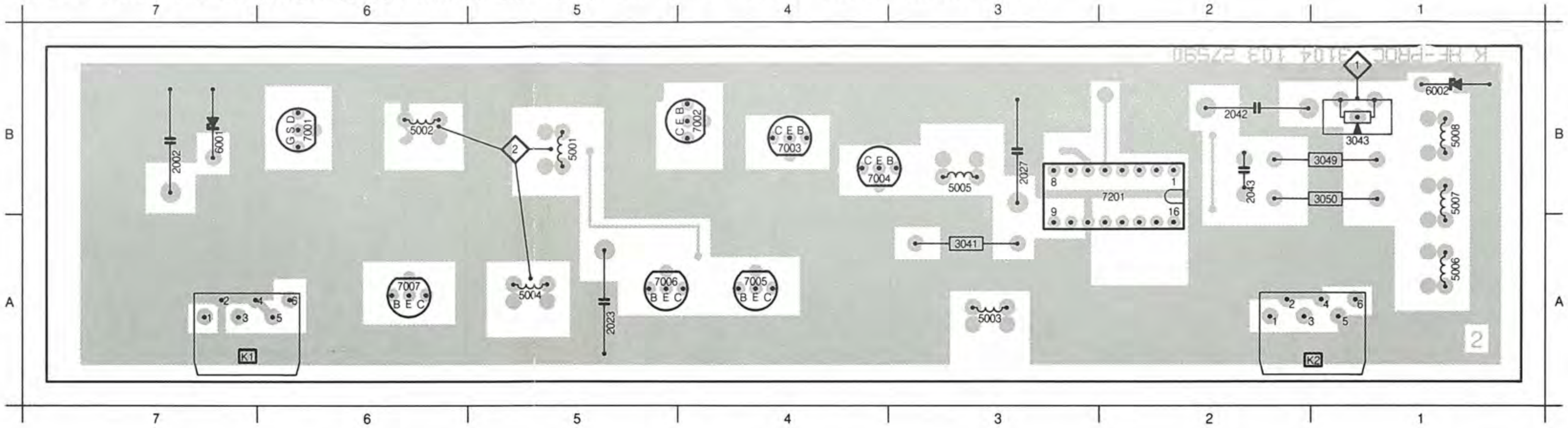
1) **R3043** (Video amplitude)
   - Using the scope, measure the CVBS OUT–signal on BNC3 (rear), 75Ω terminated.
   - Switch SK2 on Analog I/O module U in pos. NOT ENCODED (pressed).
   - Adjust R3043 until this signal is 1 Vpp ± 50 mV
   - Switch SK2 back into the earlier position.

2) **L5001, L5002, L5004** (Audio dip 0,875 MHz, MTF, Audio dip 2,8 MHz)
   - Switch the drive into STANDBY mode.
   - Connect an HF generator signal with an amplitude of 0.8 Vpp to 3K2.
   - Measure the signal on 5–IC7201–2A with the scope.
   - Set the generator to a frequency of 875 kHz and adjust L5001 for minimum amplitude of the scope signal.
   - Set the generator to a frequency of 8 MHz and an amplitude of 40 mV and adjust L5002 for maximum amplitude of the scope signal.
   - Measure the signal on 1K1 (HF–AUD) with the scope.
   - Set the generator to a frequency of 2.8 MHz and an amplitude of 20 mV and adjust L5004 for minimum amplitude of the scope signal.

Adjustment when item replaced

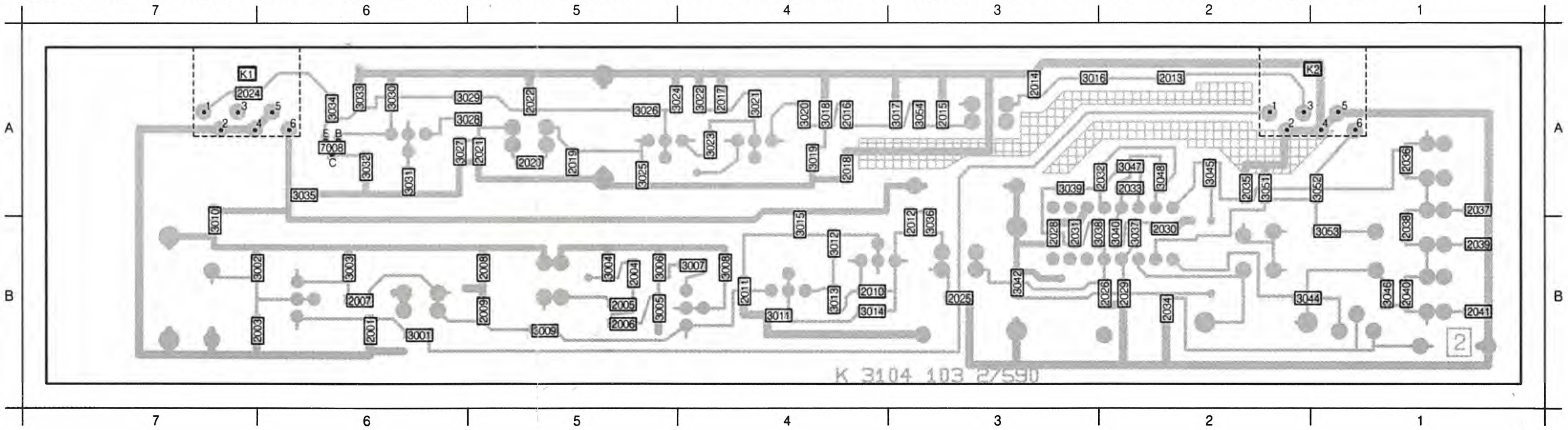
replaced	adjust
IC7201	R3043

2002 B 7	2027 B 3	2043 A 2	3043 B 1	3050 B 2	5002 B 6	5004 A 5	5006 A 1	5008 B 1	6002 B 1	7002 B 4	7004 B 4	7006 A 5	7201 B 3
2023 A 5	2042 B 2	3041 A 3	3049 B 2	5001 B 5	5003 A 3	5005 B 3	5007 A 1	6001 B 7	7001 B 6	7003 B 4	7005 A 4	7007 A 6	



2001 B 6	2007 B 6	2012 B 3	2017 A 4	2022 A 5	2029 B 2	2034 B 2	2039 B 1	3003 B 6	3008 B 4	3013 B 4	3018 A 4	3023 A 4	3028 A 6	3033 A 6
2003 B 6	2008 B 5	2013 A 2	2018 A 4	2024 A 7	2030 B 2	2035 A 2	2040 B 1	3004 B 5	3009 B 5	3014 B 4	3019 A 4	3024 A 4	3029 A 6	3034 A 6
2004 B 5	2009 B 5	2014 A 3	2019 A 5	2025 B 3	2031 B 3	2036 A 1	2041 B 1	3005 B 5	3010 A 7	3015 B 4	3020 A 4	3025 A 5	3030 A 6	3035 A 6
2005 B 5	2010 B 4	2015 A 3	2020 A 5	2026 B 2	2032 A 2	2037 A 1	3001 B 6	3006 B 5	3011 B 4	3016 A 3	3021 A 4	3026 A 5	3031 A 6	3036 B 3
2006 B 5	2011 B 4	2016 A 4	2021 A 5	2028 B 3	2033 A 2	2038 B 1	3002 B 6	3007 B 5	3012 B 4	3017 A 3	3022 A 4	3027 A 5	3032 A 6	3037 B 2

3038 B 2	3045 A 2	3052 A 1
3039 A 3	3046 B 1	3053 B 2
3040 B 2	3047 A 2	3054 A 3
3042 B 3	3048 A 2	7008 A 6
3044 B 2	3051 A 2	



PCB.01007
T10 718

LIST OF ELECTRICAL PARTS MODULE K

Coils

5001	4822 156 10994	87 μH
5002	4822 156 21147	7.2 μH
5003	4822 156 11011	2.6 μH
5004	4822 156 10994	87 μH
5005	4822 156 10999	4.2 μH
5006	4822 156 21026	34 μH
5007	4822 157 52871	25 μH
5008	4822 157 52871	25 μH

Potentiometers

3043	5322 101 10481	1 kΩ

Fuse Resistors

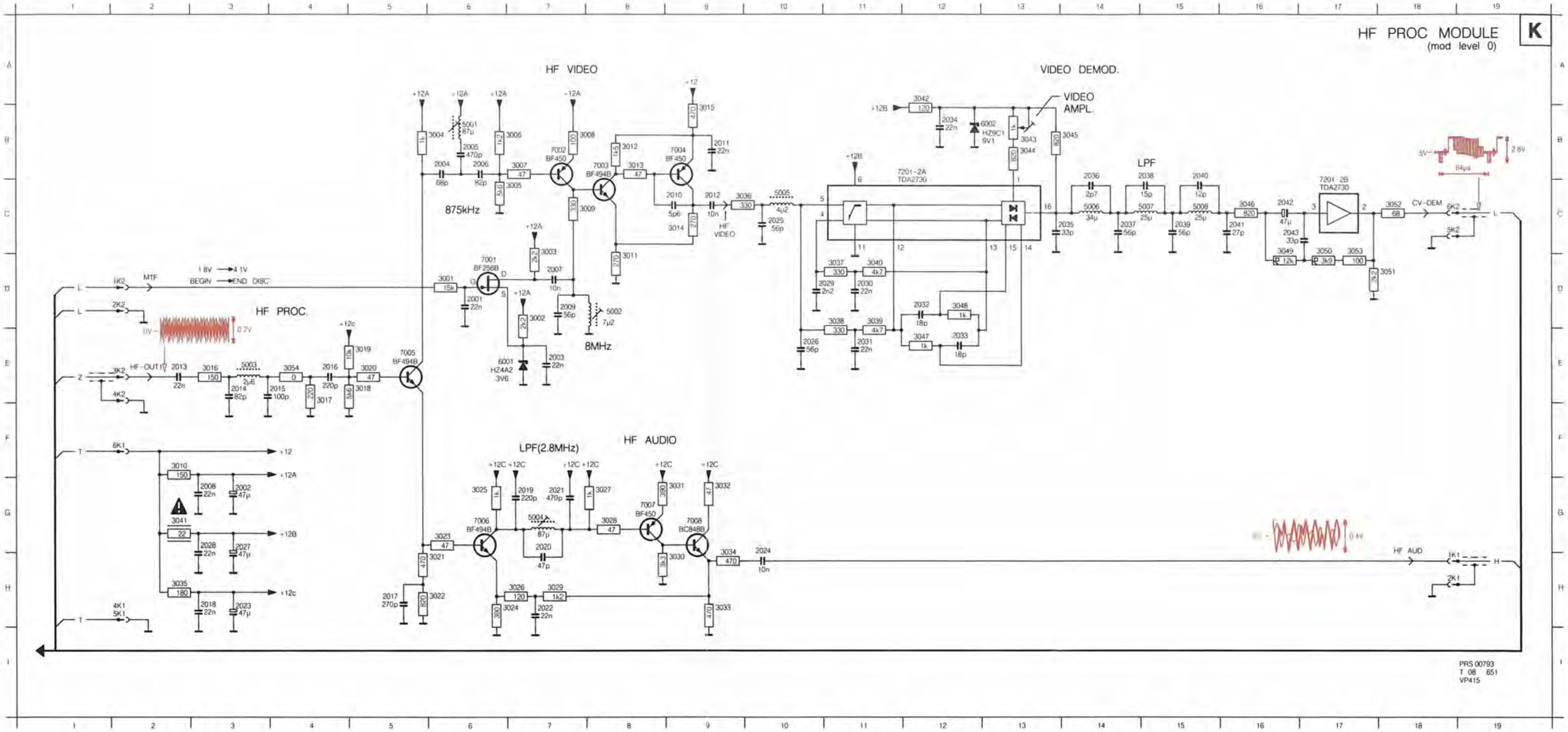
3041	4822 111 30847	22 Ω

2001	4822 122 31759	22 nF	
2002	4822 124 22027	47 μF	25 V
2003	4822 122 31759	22 nF	
2004	4822 122 33002	68 pF	
2005	4822 122 31727	470 pF	
2006	4822 122 31839	82 pF	
2007	4822 122 32442	10 nF	
2008	4822 122 31759	22 nF	
2009	4822 122 31774	56 pF	
2010	4822 122 32506	5.6 pF	
2011	4822 122 31759	22 nF	
2012	4822 122 32442	10 nF	
2013	4822 122 31759	22 nF	
2014	4822 122 31839	82 pF	
2015	4822 122 32974	100 pF	
2016	4822 122 31965	220 pF	
2017	4822 122 32142	270 pF	
2018	4822 122 31759	22 nF	
2019	4822 122 31965	220 pF	
2020	4822 122 31772	47 pF	
2021	4822 122 32976	470 pF	
2022	4822 122 31759	22 nF	
2023	4822 124 22027	47 μF	25 V
2024	4822 122 32442	10 nF	
2025	4822 122 31774	56 pF	
2026	4822 122 31774	56 pF	
2027	4822 124 22027	47 μF	25 V
2028	4822 122 31759	22 nF	
2029	4822 122 31644	2.2 nF	
2030	4822 122 31759	22 nF	
2031	4822 122 31759	22 nF	
2032	4822 122 31769	18 pF	
2033	4822 122 31769	18 pF	
2034	4822 122 31759	22 nF	
2035	4822 122 32975	33 pF	
2036	4822 122 32505	2.7 pF	
2037	4822 122 31774	56 pF	
2038	4822 122 32504	15 pF	
2039	4822 122 31774	56 pF	
2040	4822 122 32139	12 pF	
2041	4822 122 31966	27 pF	
2042	4822 124 22027	47 μF	25 V
2043	5322 122 32072	33 pF	

2001	D 6	2006	B 5	2011	B 9	2016	E 4	2021	G 7	2026	E10	2031	E11	2036	B14
2002	G 3	2007	D 7	2012	C 9	2017	H 5	2022	H 7	2027	G 3	2032	D12	2037	C14
2003	E 7	2008	G 3	2013	E 2	2018	H 3	2023	H 3	2028	G 3	2033	E12	2038	B15
2004	B 6	2009	D 7	2014	E 3	2019	G 7	2024	G10	2029	D11	2034	B12	2039	C15
2005	B 6	2010	C 9	2015	E 4	2020	G 7	2025	C10	2030	D11	2035	C14	2040	B15

2041	C16	3003	C 7	3008	B 8	3013	B 8	3018	E 5	3023	G 6	3028	G 8	3033	H 9
2042	C16	3004	B 6	3009	C 8	3014	C 9	3019	E 5	3024	H 7	3029	H 7	3034	G 9
2043	C16	3005	C 7	3010	F 2	3015	B 9	3020	E 5	3025	G 6	3030	H 9	3035	H 2
3001	D 6	3006	B 7	3011	D 8	3016	E 3	3021	H 6	3026	H 7	3031	G 9	3036	C 9
3002	D 7	3007	B 7	3012	B 8	3017	E 4	3022	H 6	3027	G 8	3032	G 9	3037	D11

3038	D11	3043	B13	3048	D12	3053	C17	5004	G 7	6001	E 7	7004	B 9	7201	C17
3039	D11	3044	B13	3049	C16	3054	E 4	5005	C10	6002	B13	7005	E 5	7201	B12
3040	D11	3045	B14	3050	C17	5001	B 6	5006	C14	7001	D 6	7006	G 6		
3041	G 2	3046	C16	3051	D18	5002	D 8	5007	C15	7002	B 7	7007	G 8		
3042	A12	3047	E12	3052	C18	5003	E 3	5008	C15	7003	B 8	7008	G 9		



2001	B 6	2008	F 7	2015	G21	2022	M 5	2029	J 9	2036	M 7	3004	B 3
2002	A 8	2009	F 8	2016	H20	2023	I 4	2030	J 8	2037	M 8	3005	B 5
2003	B12	2010	G15	2017	K 3	2024	L 7	2031	J 7	2038	N 8	3006	C 5
2004	B13	2011	G15	2018	K 4	2025	L 6	2032	K11	2039	N 9	3007	B 5
2005	B13	2012	G16	2019	K 5	2026	K 6	2033	H11	3001	B 2	3008	A 5
2006	F 4	2013	H16	2020	K 5	2027	L 7	2034	N 6	3002	B 3	3009	B 5
2007	F 6	2014	G19	2021	L 6	2028	J 9	2035	M 6	3003	B 3	3010	C 5

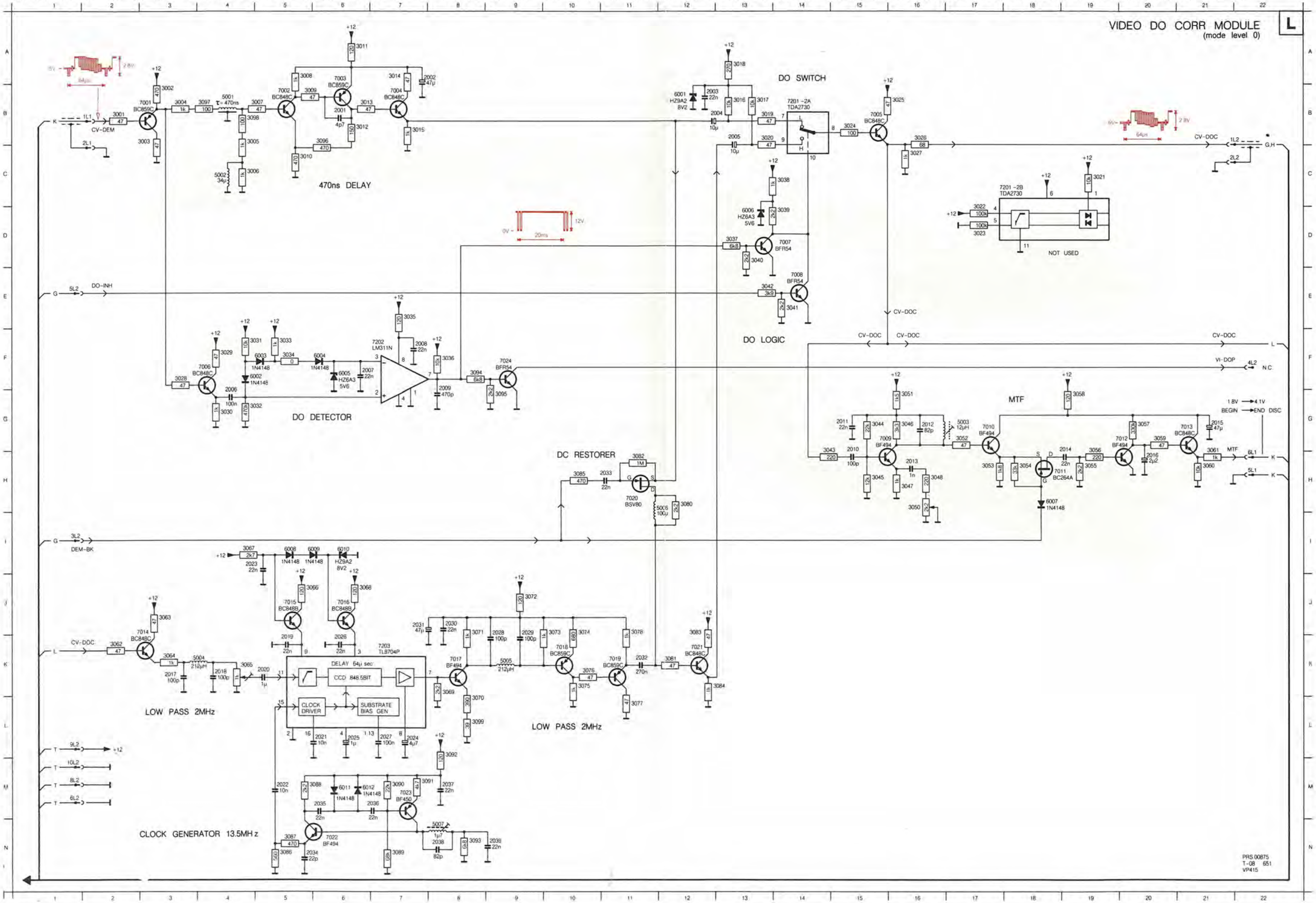
3011	A 6	3018	A13	3025	B16	3032	G 5	3039	D14	3046	G16	3054	H18
3012	B 6	3019	B13	3026	B16	3033	F 5	3040	D13	3047	H16	3055	H19
3013	B 6	3020	B13	3027	C16	3034	F 5	3041	E14	3048	H16	3056	G19
3014	A 7	3021	C19	3028	F 3	3035	E 7	3042	E13	3050	H16	3057	G20
3015	B 7	3022	C17	3029	F 4	3036	F 8	3043	G14	3051	G16	3058	G19
3016	B13	3023	D17	3030	G 4	3037	D13	3044	G15	3052	G17	3059	G20
3017	B13	3024	B15	3031	F 5	3038	C14	3045	H15	3053	H17	3060	H21

3061	G21	3068	J 6	3075	K10	3083	J12	3090	M 7	3097	B 4	5005	K 9
3062	K 2	3069	K 8	3076	K10	3084	K13	3091	M 8	3098	B 5	5006	H12
3063	J 3	3070	L 8	3077	L11	3085	H10	3092	L 6	3099	L 8	5007	N 8
3064	K 3	3071	J 8	3078	J11	3086	N 5	3093	N 8	5001	B 4	6001	B12
3065	K 4	3072	J 9	3080	H12	3087	N 5	3094	F 8	5002	C 4	6002	F 5
3066	J 6	3073	J10	3081	K12	3088	M 6	3095	G 9	5003	G17	6003	F 5
3067	I 4	3074	J10	3082	H11	3089	N 7	3096	B 6	5004	K 4	6004	F 6

6005	F 6	6012	M 7	7007	D14	7014	J 3	7021	K12	7203	K 7		
6006	D13	7001	B 3	7008	E14	7015	J 5	7022	N 6				
6007	H18	7002	B 5	7009	G15	7016	J 6	7023	M 7				
6008	I 5	7003	A 6	7010	G17	7017	K 8	7024	F 9				
6009	I 6	7004	B 7	7011	H19	7018	K10	7201	C18				
6010	I 6	7005	B15	7012	G20	7019	K11	7201	B14				
6011	M 6	7006	F 4	7013	G21	7020	H11	7202	F 7				

VIDEO DO CORR MODULE
(mode level 0)

L



CS 6 878

VIDEO DO CORR MODULE L

(MOD LEVEL 0)

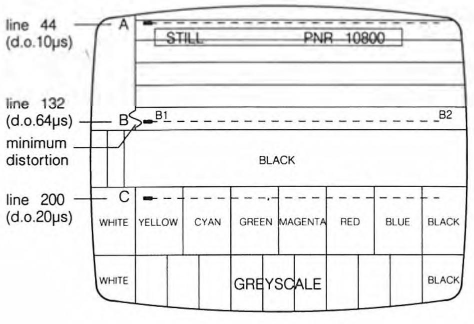
ADJUSTMENTS

Required
Scope
Test disc

Adjustment conditions
Load test disc.
Still picture, picture no. 10800.

Adjustments

1) **R3065, L5007** (Delay 64 µs)
   - Picture no. 10800 is visible on the picture screen as shown in fig. L1.



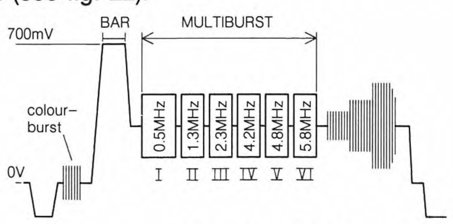
DROP OUT SIGNALS

Fig. L1

MDA.00588
T28/711

   - Adjust L5007 until drop-out A gives a white completion of the vertical lines at the right place and drop-out B gives minimum distortion at the place indicated.
   - Adjust R3065 until drop-out B is invisible and drop-out C causes a black line without any white stripes or dots.

2) **L5003, R3050** (MTF)
   - Search for picture no. 1000 (blue).
   - Using the scope, measure the CVBS OUT-signal on BNC3 (rear), 75Ω terminated, triggered line frequent.
   - Switch SK2 on Analog I/O module U in pos. NOT ENCODED (pressed).
   - Adjust L5003 for min. amplitude of the chroma signal.
   - Measure the CVBS OUT-signal (NOT ENCODED) on BNC3 with the scope and search the multi-burst signal in the VITS (line 20) by means of the delayed time base (see fig. L2).



VITS SIGNALS LINE 20

Fig. L2

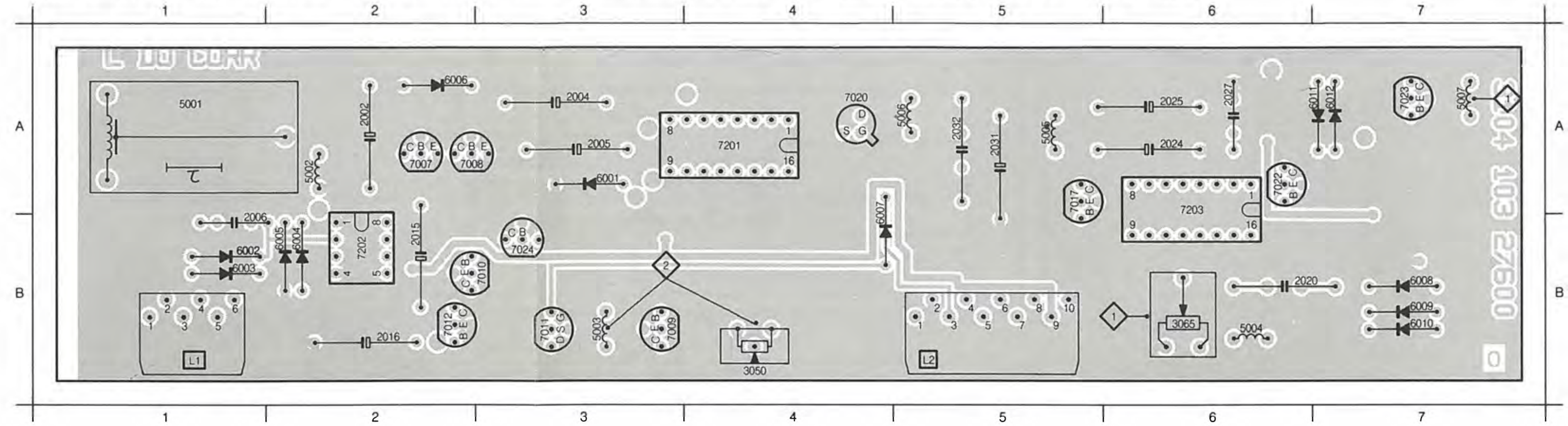
MDA.00588
T28/711

   - Adjust R3050 until the amplitude of MBI = MBIV.

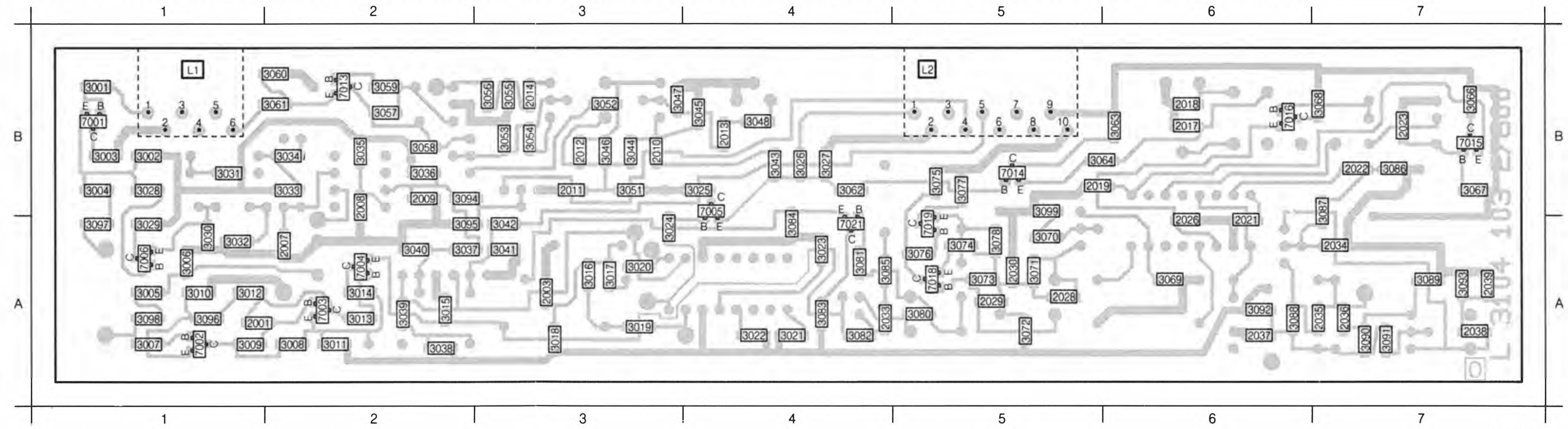
Adjustment when item replaced

replaced	adjust
Components in CLOCK GEN.	L5007
IC7203	R3065, R3050

2002 A 2	2006 B 1	2020 B 6	2027 A 6	3050 B 4	5003 B 3	5006 A 5	6002 B 1	6005 B 2	6008 B 7	6011 A 7	7008 A 3	7011 B 3	7020 A 4	7024 B 3	7203 A 6
2004 A 3	2015 B 2	2024 A 6	2031 A 5	3065 B 6	5004 B 6	5007 A 7	6003 B 1	6006 A 2	6009 B 7	6012 A 7	7009 B 3	7012 B 2	7022 A 6	7201 A 4	
2005 A 3	2016 B 2	2025 A 6	2032 A 5	5002 A 2	5005 A 5	6001 A 3	6004 B 2	6007 A 4	6010 B 7	7007 A 2	7010 B 3	7017 A 5	7023 A 7	7202 B 2	



2001 A 1	2013 B 4	2026 A 6	2037 A 6	3006 A 1	3014 A 2	3022 A 4	3030 A 1	3038 A 2	3046 B 3	3056 B 3	3064 B 6	3073 A 5	3082 A 4	3090 A 7	3098 A 1	7013 B 2
2003 A 3	2014 B 3	2028 A 5	2038 A 7	3007 A 1	3015 A 2	3023 A 4	3031 B 1	3039 A 2	3047 B 3	3057 B 2	3066 B 7	3074 A 5	3083 A 4	3091 A 7	3099 A 5	7014 B 5
2007 A 2	2017 B 6	2029 A 5	2039 A 7	3008 A 2	3016 A 3	3024 A 3	3032 A 1	3040 A 2	3048 B 4	3058 B 2	3067 B 7	3075 B 5	3084 A 4	3092 A 6	7001 B 1	7015 B 7
2008 A 2	2018 B 6	2030 A 5	3001 B 1	3009 A 1	3017 A 3	3025 B 4	3033 B 2	3041 A 3	3051 B 3	3059 B 2	3068 B 7	3076 A 5	3085 A 4	3093 A 7	7002 A 1	7016 B 6
2009 B 2	2019 B 5	2033 A 4	3002 B 1	3010 A 1	3018 A 3	3026 B 4	3034 B 2	3042 A 3	3052 B 3	3060 B 2	3069 A 6	3077 A 5	3086 B 7	3094 B 2	7003 A 2	7018 A 5
2010 B 3	2021 A 6	2034 A 7	3003 B 1	3011 A 2	3019 A 3	3027 B 4	3035 B 2	3043 B 4	3053 B 3	3061 B 2	3070 A 5	3078 A 5	3087 A 7	3095 A 2	7004 A 2	7019 A 5
2011 B 3	2022 B 7	2035 A 7	3004 B 1	3012 A 1	3020 A 3	3028 B 1	3036 B 2	3044 B 3	3054 B 3	3062 B 4	3071 A 5	3080 A 5	3088 A 6	3096 A 1	7005 A 4	7021 A 4
2012 B 3	2023 B 7	2036 A 7	3005 A 1	3013 A 2	3021 A 4	3029 A 1	3037 A 2	3045 B 4	3055 B 3	3063 B 6	3072 A 5	3081 A 4	3089 A 7	3097 A 1	7006 A 1	



PCB 01008
T10 718

LIST OF ELECTRICAL PARTS MODULE L

Delay lines

5001	4822 320 40081	DL470NS

Coils

5002	4822 157 52869	34 µH
5003	4822 156 11003	12 µH
5004	4822 156 11007	212 µH
5005	4822 156 11007	212 µH
5006	4822 156 21324	100 µH
5007	4822 156 10997	1.7 µH

Potentiometers

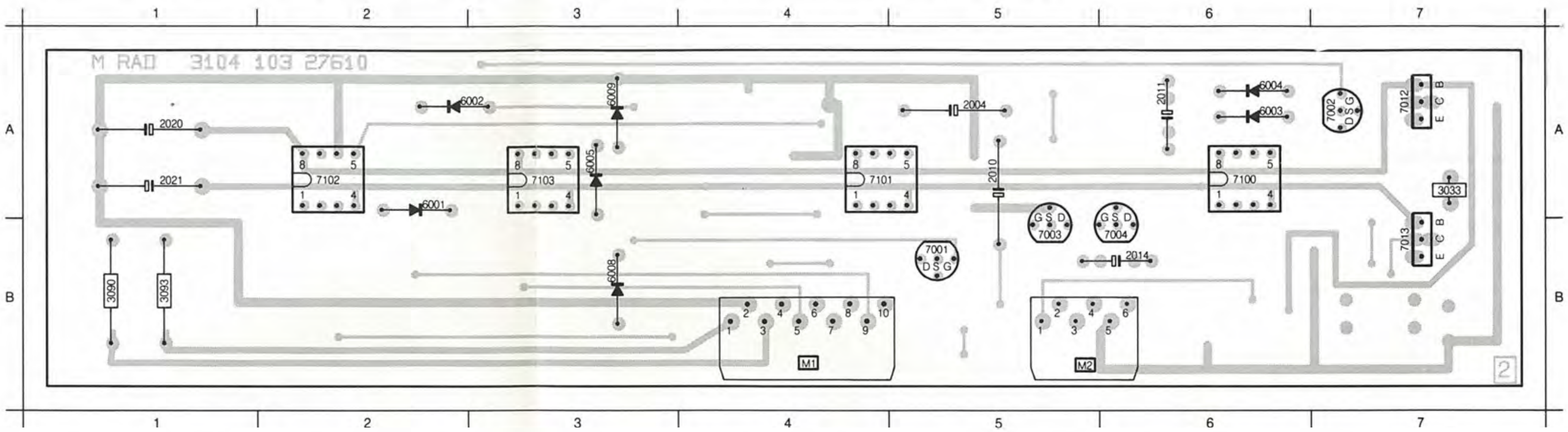
3050	4822 100 11087	2.2 kΩ
3065	4822 100 20151	1 kΩ

2001	4822 122 32082	4.7 pF	
2002	4822 124 22027	47 µF	25 V
2003	4822 122 31759	22 nF	
2004	5322 124 21749	10 µF	63 V
2005	5322 124 21749	10 µF	63 V
2006	4822 121 41608	100 nF	100 V
2007	4822 122 31759	22 nF	
2008	4822 122 31759	22 nF	
2009	4822 122 32976	470 pF	
2010	4822 122 32974	100 pF	
2011	4822 122 31759	22 nF	
2012	4822 122 31839	82 pF	
2013	5322 122 31647	1 nF	
2014	4822 122 31759	22 nF	
2015	4822 124 22027	47 µF	25 V
2016	4822 124 22029	2.2 µF	63 V
2017	4822 122 32974	100 pF	
2018	4822 122 32974	100 pF	
2019	4822 122 31759	22 nF	
2020	4822 121 41719	1 µF	10% 100 V
2021	4822 122 32442	10 nF	
2022	4822 122 32442	10 nF	
2023	4822 122 31759	22 nF	
2024	4822 124 22031	4.7 µF	63 V
2025	4822 124 22028	1 µF	63 V
2026	4822 122 31759	22 nF	
2027	4822 121 41608	100 nF	100 V
2028	4822 122 32974	100 pF	
2029	4822 122 32974	100 pF	
2030	4822 122 31759	22 nF	
2031	4822 124 22027	47 µF	25 V
2032	4822 121 41785	270 nF	10% 100 V
2033	4822 122 31759	22 nF	
2034	4822 122 32482	22 pF	
2035	4822 122 31759	22 nF	
2036	4822 122 31759	22 nF	
2037	4822 122 31759	22 nF	
2038	4822 122 31839	82 pF	
2039	4822 122 31759	22 nF	

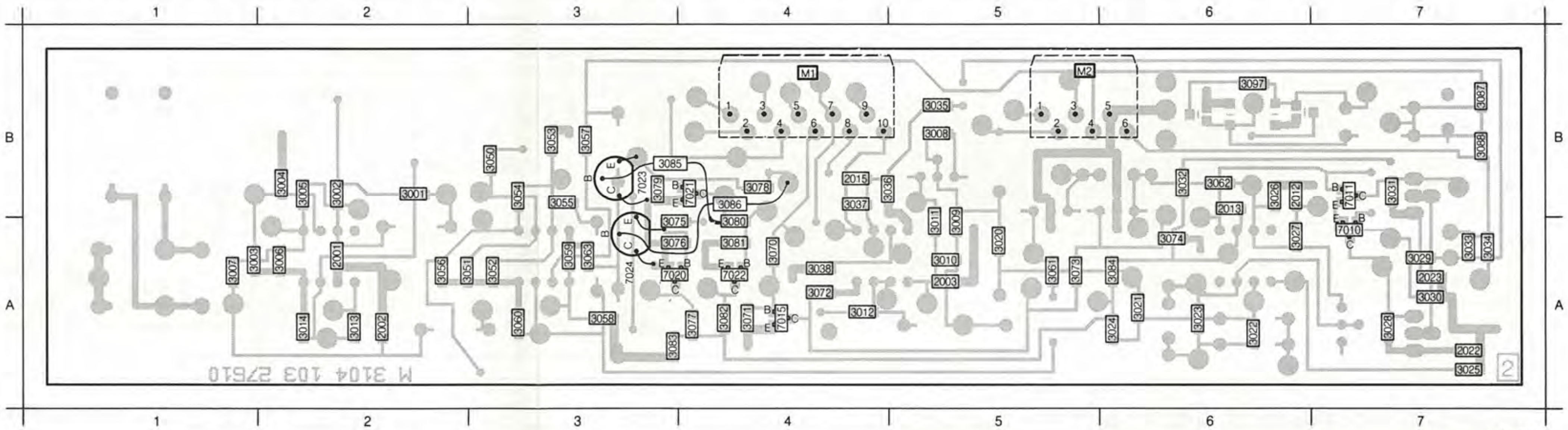
RADIAL MODULE M

(MOD. LEVEL 1)

2004 A 5	2011 A 6	2020 A 1	3033 A 7	3093 B 1	6002 A 3	6004 A 6	6008 B 3	7001 B 5	7002 A 7	7003 B 5	7004 B 6	7013 B 7
2010 A 5	2014 B 6	2021 A 1	3090 B 1	6001 A 2	6003 A 6	6005 A 3	6009 A 3	7101 A 4	7102 A 2	7103 A 3	7012 A 7	7100 A 6



2001 A 2	2015 B 4	3003 A 1	3008 B 5	3013 A 2	3023 A 6	3028 A 7	3033 A 7	3038 A 4	3054 A 3	3059 A 3	3070 A 4	3075 A 4	3080 A 4	3085 B 3	7010 A 7	7022 A 4
2002 A 2	2022 A 7	3004 B 2	3009 A 5	3014 A 2	3024 A 6	3029 A 7	3034 A 7	3050 B 3	3055 B 3	3060 A 3	3071 A 4	3076 A 4	3081 A 4	3086 B 4	7011 A 7	7023 B 3
2003 A 5	2023 A 7	3005 A 2	3010 A 5	3020 A 5	3025 A 7	3030 A 7	3035 B 5	3051 A 2	3056 A 2	3061 A 5	3072 A 4	3077 A 4	3082 A 4	3087 B 7	7015 A 4	7024 A 3
2012 A 6	3001 B 2	3006 A 2	3011 A 5	3021 A 6	3026 A 6	3031 A 7	3036 B 4	3052 A 3	3057 B 3	3062 B 6	3073 A 5	3078 B 4	3083 A 3	3088 B 7	7020 A 4	
2013 B 6	3002 A 2	3007 A 1	3012 A 4	3022 A 6	3027 A 6	3032 B 6	3037 B 4	3053 B 3	3058 A 3	3063 A 3	3074 A 6	3079 B 3	3084 A 6	3097 B 6	7021 A 4	



PCB 01009
T03/715

LIST OF ELECTRICAL PARTS MODULE M

PTC Resistors

3033	4822 116 40026	5.6 Ω

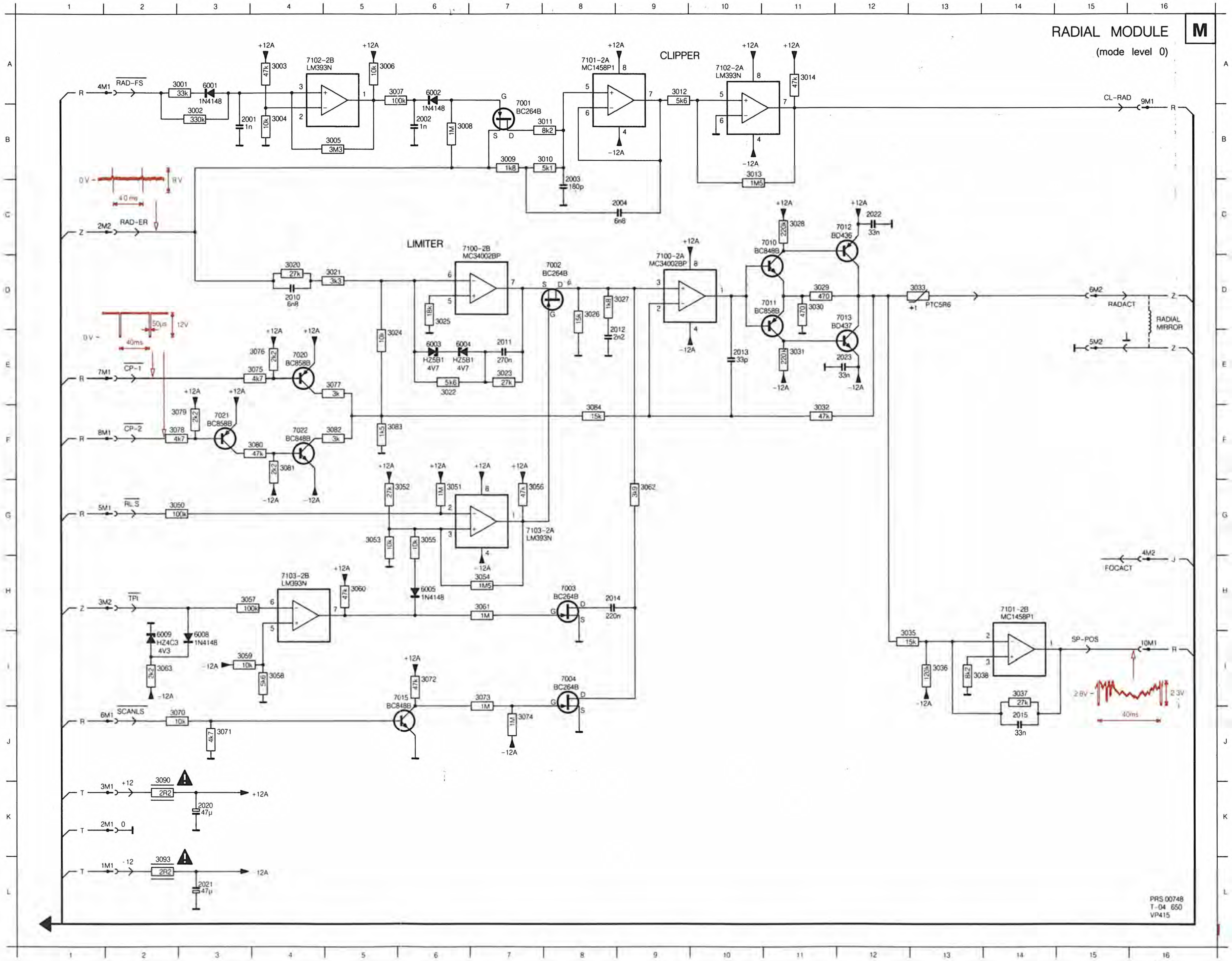
NFR Resistors

3090	4822 111 30492	2.2 Ω
3093	4822 111 30492	2.2 Ω

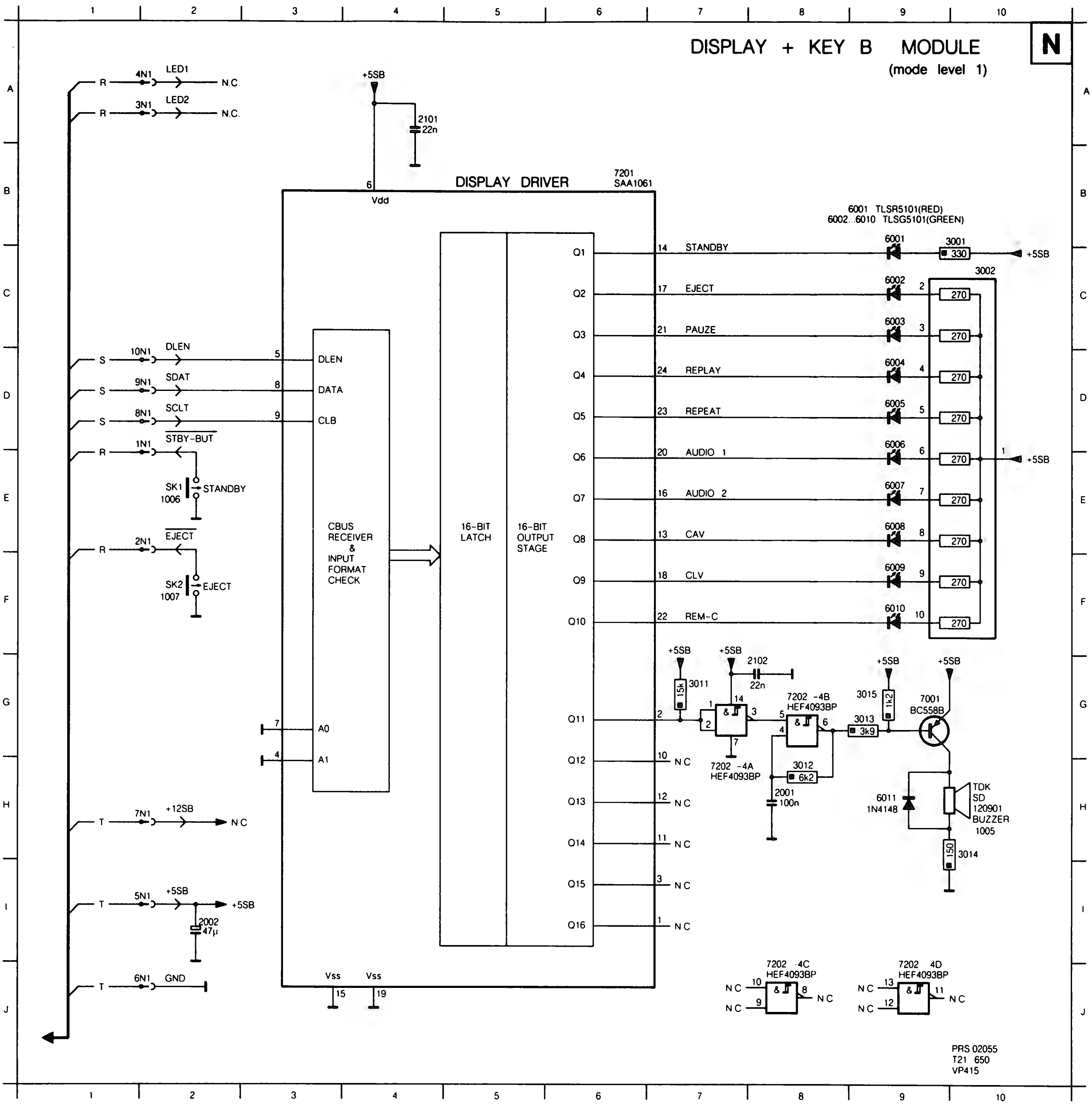
2001	5322 122 31647	1 nF	
2002	5322 122 31647	1 nF	
2003	4822 122 31768	180 pF	
2004	4822 121 50538	6.8 nF	63 V
2010	4822 121 50538	6.8 nF	63 V
2011	4822 121 41874	270 nF	63 V
2012	4822 122 31644	2.2 nF	
2013	4822 122 32975	33 pF	
2014	4822 121 41876	220 nF	20% 63 V
2015	5322 122 31848	33 nF	
2020	4822 124 22027	47 µF	25 V
2021	4822 124 22027	47 µF	25 V
2022	5322 122 31848	33 nF	
2023	5322 122 31848	33 nF	

2001	B 4	2012	D 9	2022	C12	3005	B 5	3011	B 8	3022	E 6	3028	C11	3035	I 12	3052	G 6
2002	B 6	2013	E10	2023	E12	3006	A 5	3012	A 9	3023	E 7	3029	D11	3036	I 13	3053	G 5
2003	B 8	2014	H 8	3001	A 3	3007	A 6	3013	B10	3024	E 6	3030	D11	3037	I 14	3054	H 7
2004	C 9	2015	J14	3002	B 3	3008	B 6	3014	A11	3025	D 6	3031	E11	3038	I 14	3055	G 6
2010	D 4	2020	K 3	3003	A 4	3009	B 7	3020	D 4	3026	D 8	3032	F11	3050	G 2	3056	G 7
2011	E 7	2021	L 3	3004	B 4	3010	B 8	3021	D 5	3027	D 9	3033	D13	3051	G 6	3057	H 3

3058	I 4	3070	J 2	3076	E 4	3082	F 5	6002	A 6	7001	A 7	7012	C12	7100	C 7	7103	G 7
3059	I 3	3071	J 3	3077	E 5	3083	F 6	6003	E 6	7002	D 8	7013	D12	7100	D 9	7103	H 4
3060	H 5	3072	I 6	3078	F 2	3084	F 8	6004	E 6	7003	H 8	7015	I 6	7101	A 8		
3061	H 7	3073	I 7	3079	F 3	3090	J 2	6005	H 6	7004	I 8	7020	E 4	7101	H14		
3062	G 9	3074	J 7	3080	F 4	3093	L 2	6008	I 3	7010	C11	7021	F 3	7102	A 4		
3063	I 2	3075	E 4	3081	F 4	6001	A 3	6009	I 2	7011	D11	7022	F 4	7102	A10		



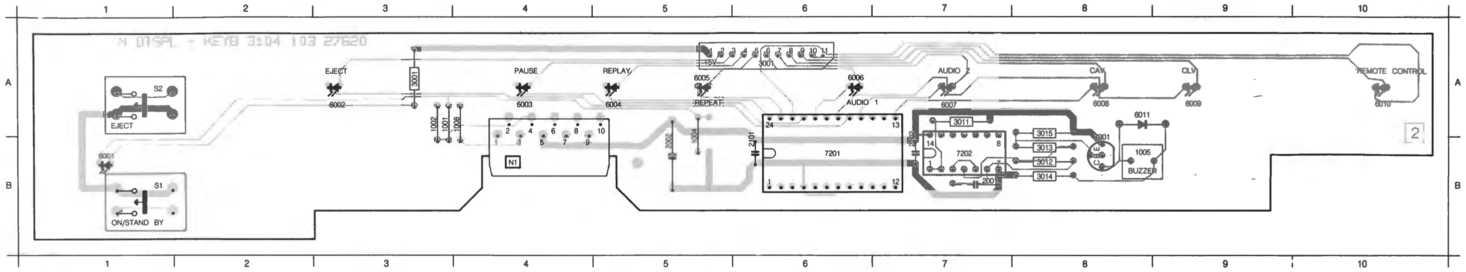
1005	H10	2001	H 8	2102	G 8	3011	G 7	3014	H10	6002	C 9	6005	D 9	6008	E 9	6011	H 9	7202	J 8	7202	H 7
1006	E 2	2002	I 2	3001	B10	3012	H 8	3015	G 9	6003	C 9	6006	D 9	6009	F 9	7001	G 9	7202	J 9		
1007	F 2	2101	A 4	3002	C10	3013	G 9	6001	B 9	6004	D 9	6007	E 9	6010	F 9	7201	B 6	7202	G 8		



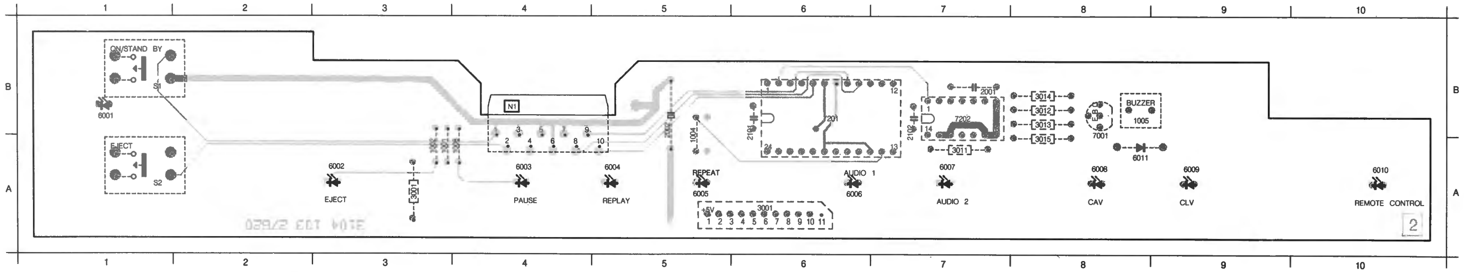
DISPLAY + KEYB. MODULE N

(MOD. LEVEL 1)

1001 A 3	1004 A 5	1008 A 4	2101 A 6	2002 B 5	3001 A 3	3012 B 8	3014 B 8	6001 B 1	6003 A 4	6005 A 5	6007 A 7	6009 A 9	6011 A 8	7201 B 6
1002 A 3	1005 B 8	2001 B 7	2102 A 7	3001 A 6	3011 A 7	3013 B 8	3015 A 8	6002 A 3	6004 A 5	6006 A 6	6008 A 8	6010 A10	7001 B 8	7202 B 7



1001 A 3	1004 A 5	1008 A 4	2101 A 6	2002 A 5	3001 A 3	3012 B 8	3014 B 8	6001 B 1	6003 A 4	6005 A 5	6007 A 7	6009 A 9	6011 A 8	7201 B 6
1002 A 3	1005 B 8	2001 B 7	2102 A 7	3001 A 6	3011 A 7	3013 B 8	3015 A 8	6002 A 3	6004 A 5	6006 A 6	6008 A 8	6010 A10	7001 A 8	7202 B 8



PCB.01010
T03/716

LIST OF ELECTRICAL PARTS MODULE N

Buzzer
1005 4822 280 10151 Buzzer SD120901

LEDs
6001 4822 130 80111 TLSR5101
6002..6010 4822 130 80113 TLSG5101

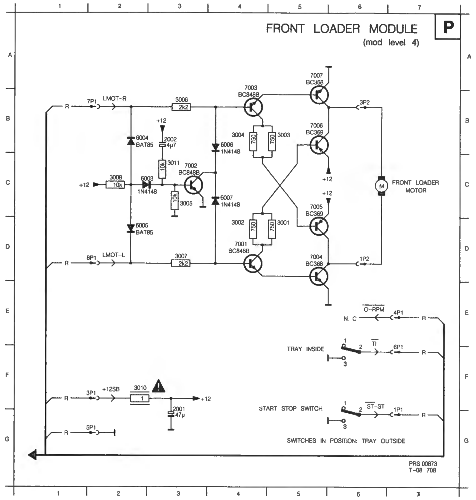
Resistor networks
3002 4822 116 90249 9x 270 Ω

2001	4822 121 41608	100 nF	100 V
2002	4822 124 22027	47 µF	25 V
2101	4822 122 30103	22 nF	63 V
2102	4822 122 30103	22 nF	63 V

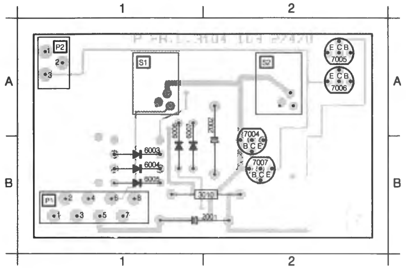
FRONTLOADER MODULE P

(MOD. LEVEL 4)

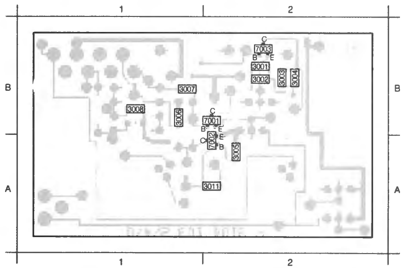
2001 F 3	3002 D 4	3005 C 3	3008 C 2	6003 C 2	6006 B 4	7002 C 3	7005 C 5
2002 B 3	3003 B 5	3006 B 3	3010 F 2	6004 B 2	6007 C 4	7003 A 4	7006 B 5
3001 D 5	3004 B 4	3007 D 3	3011 C 3	6005 D 2	7001 D 4	7004 D 5	7007 A 5



2001 B 2	3010 B 2	6004 B 1	6006 A 1	7004 A 2	7006 A 2
2002 A 2	6003 B 1	6005 B 1	6007 A 1	7005 A 2	7007 B 2



3001 B 2	3003 B 2	3005 A 2	3007 B 1	3011 A 2	7002 A 2
3002 B 2	3004 B 2	3006 A 1	3008 B 1	7001 B 2	7003 B 2



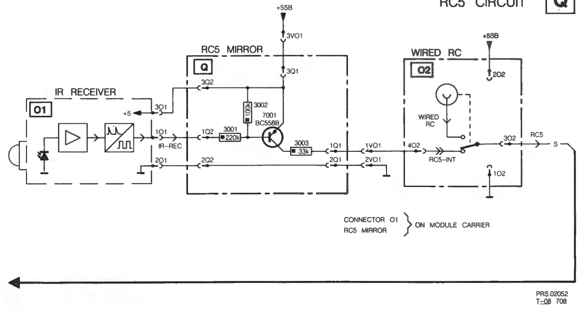
PCB.01012
T03/715

LIST OF ELECTRICAL PARTS MODULE P

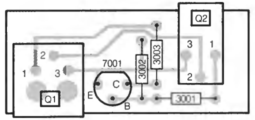
NFR25 Resistors
3010 4822 111 30483 1 Ω

2001	4822 124 22027	47 µF	25 V
2002	4822 124 22031	4.7 µF	63 V

RC5 CIRCUIT Q



RC5 MIRROR Q



PCB.01036
719

LIST OF ELECTRICAL PARTS MODULE R

Eproms (programmed)

7204	4822 209 51257	TMS 27128 drive

Crystals

5001	4822 242 71663	12 MHz

Coils

5002	4822 158 10101	5.3 µH
5003	4822 158 10101	5.3 µH
5004	4822 157 51316	120 µH

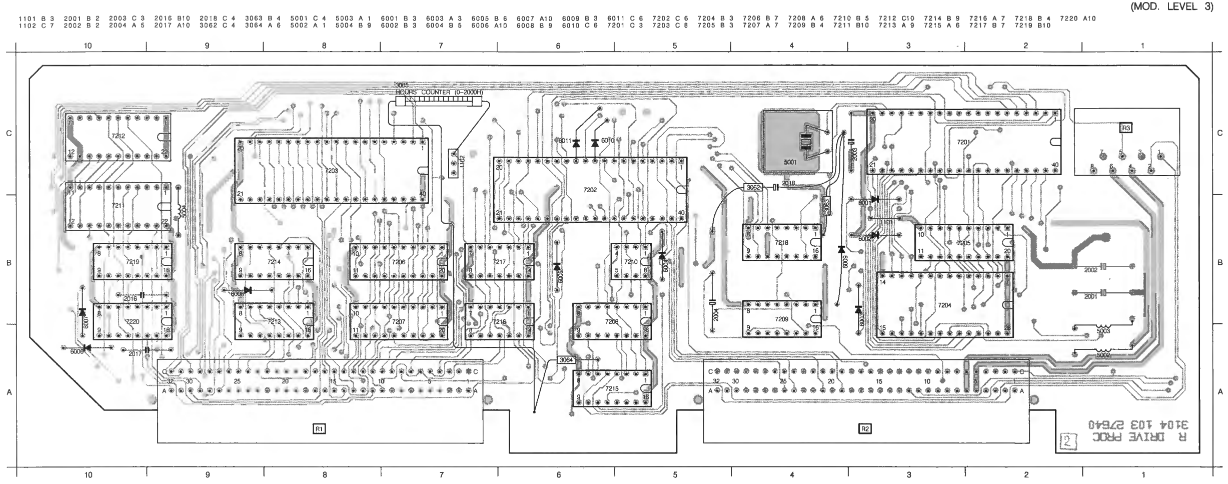
Hours counter

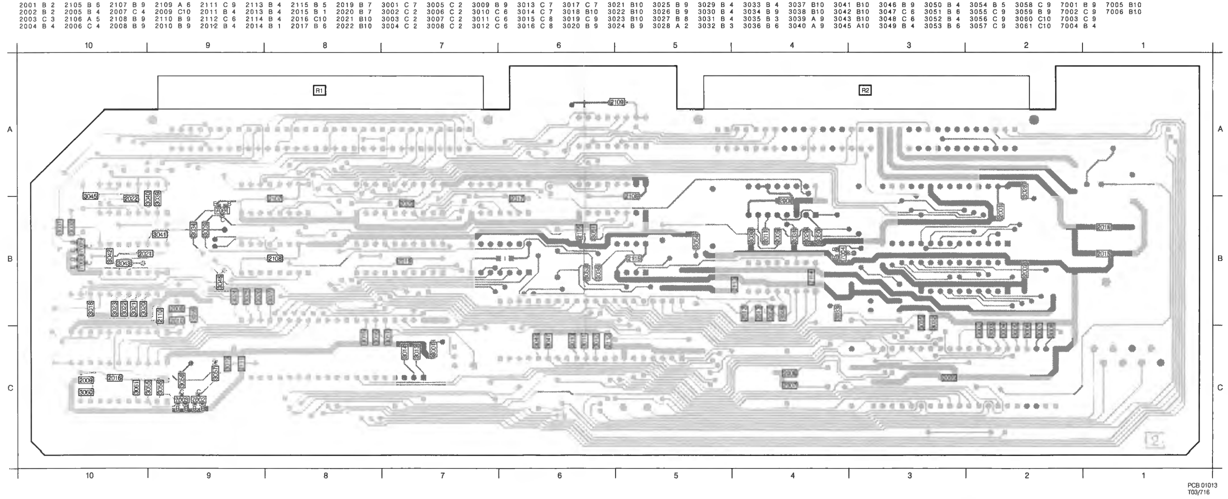
3065	4822 344 40081	Hours counter

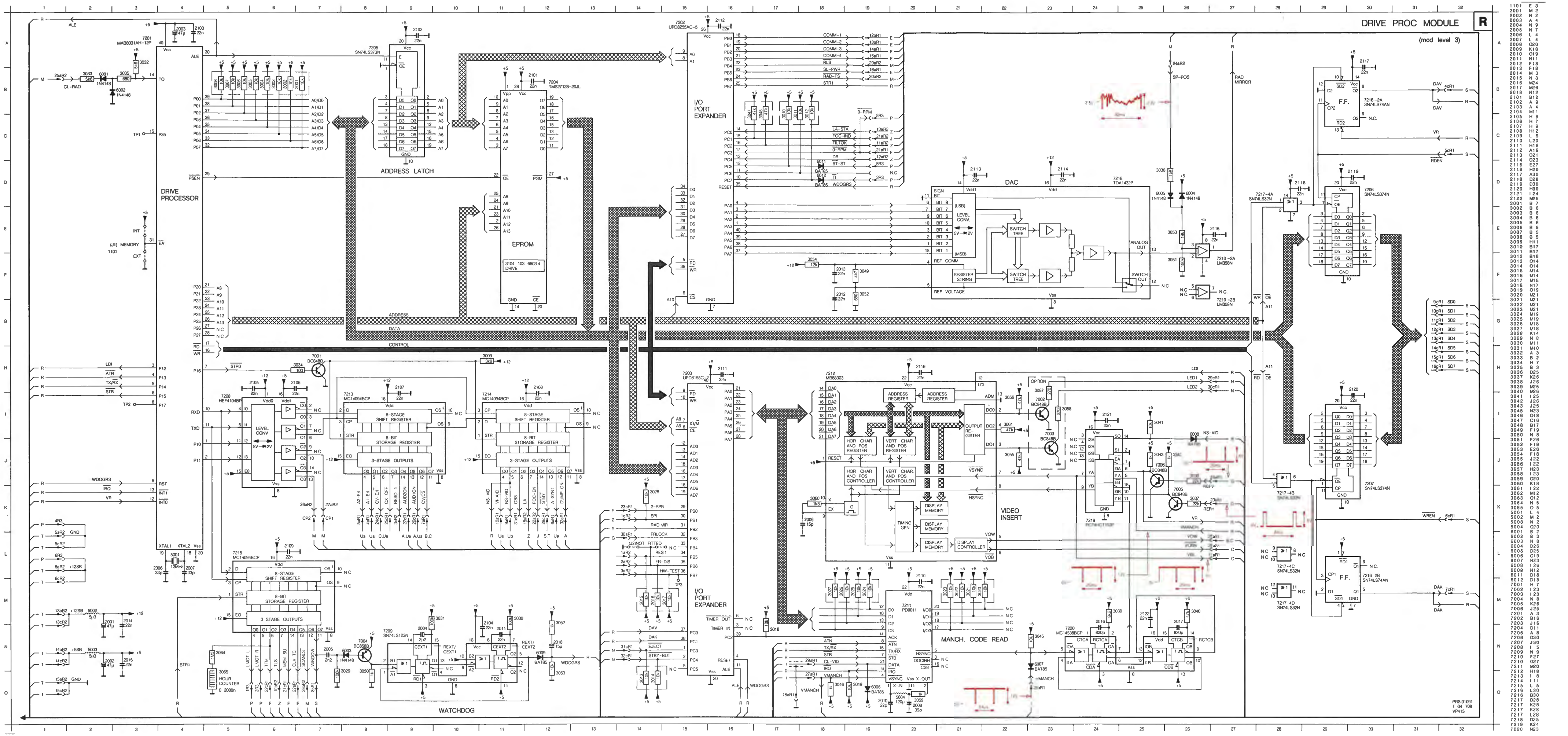
2001	4822 124 22027	47 µF	25 V
2002	4822 124 22027	47 µF	25 V
2003	4822 124 22027	47 µF	25 V
2004	4822 124 22029	2.2 µF	63 V
2005	4822 122 31644	2.2 nF	
2006	4822 122 32975	33 pF	
2007	4822 122 32975	33 pF	
2008	4822 122 31972	39 pF	
2009	4822 122 32504	15 pF	
2010	4822 122 32482	22 pF	
2011	4822 122 31759	22 nF	
2012	4822 122 31759	22 nF	
2013	4822 122 31759	22 nF	
2014	4822 122 31759	22 nF	
2015	4822 122 31759	22 nF	
2016	5322 121 54072	820 pF	250 V
2017	5322 121 54072	820 pF	250 V
2018	4822 124 22187	15 µF	63 V
2101	4822 122 31759	22 nF	
2102	4822 122 31759	22 nF	
2103	4822 122 31759	22 nF	
2104	4822 122 31759	22 nF	
2105	4822 122 31759	22 nF	
2106	4822 122 31759	22 nF	
2107	4822 122 31759	22 nF	
2108	4822 122 31759	22 nF	
2109	4822 122 31759	22 nF	
2110	4822 122 31759	22 nF	
2111	4822 122 31759	22 nF	
2112	4822 122 31759	22 nF	
2113	4822 122 31759	22 nF	
2114	4822 122 31759	22 nF	
2115	4822 122 31759	22 nF	
2116	4822 122 31759	22 nF	
2117	4822 122 31759	22 nF	
2118	4822 122 31759	22 nF	
2119	4822 122 31759	22 nF	
2120	4822 122 31759	22 nF	
2121	4822 122 31759	22 nF	
2122	4822 122 31759	22 nF	

DRIVE PROC. MODULE R

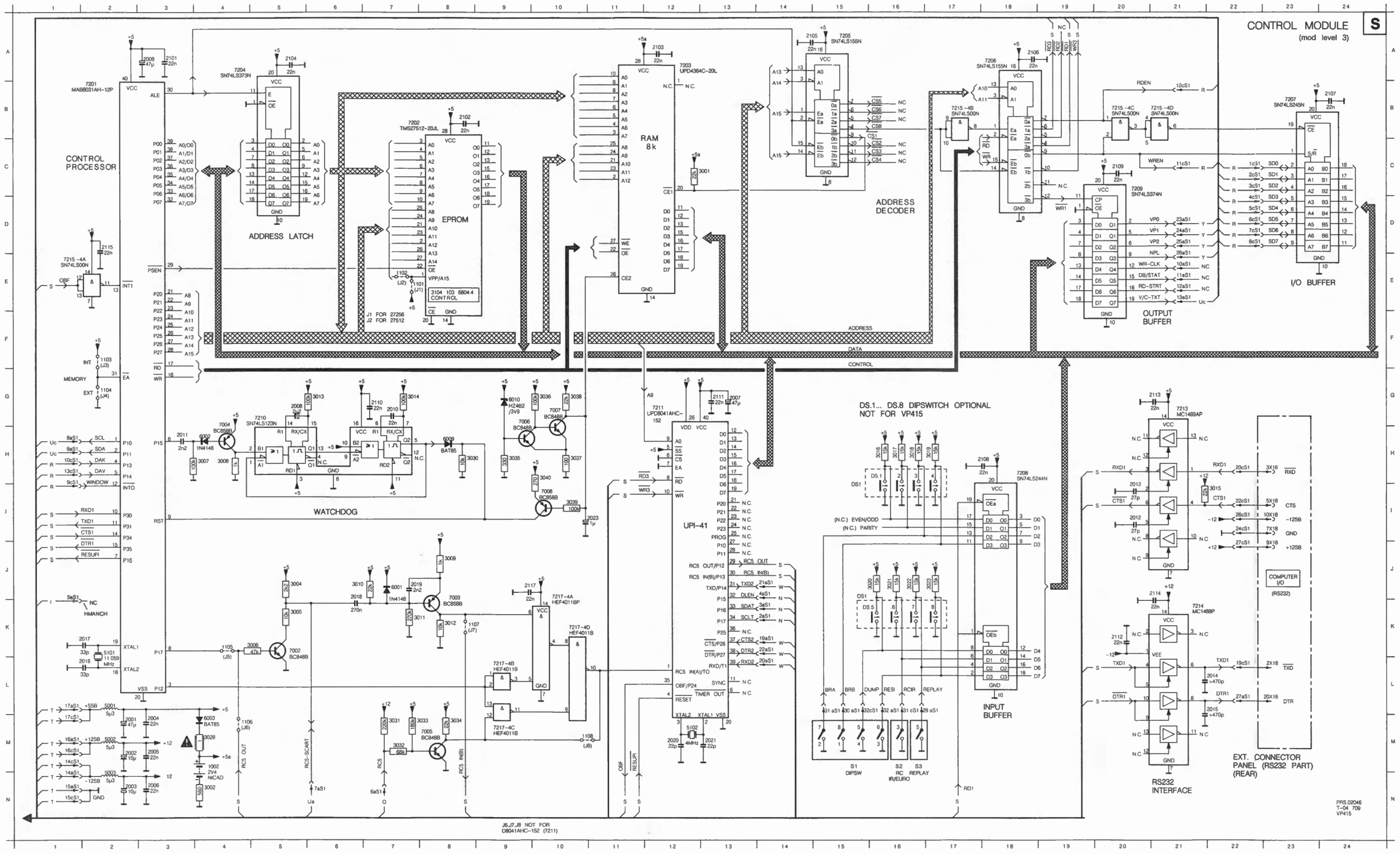
(MOD. LEVEL 3)






DRIVE PROC MODULE
(mod level 3)
R
DRIVE PROCESSOR
ADDRESS LATCH
EPROM
I/O PORT EXPANDER
DAC
ADDRESS
DATA
CONTROL
VIDEO INSERT
MANCH. CODE READ
WATCHDOG
HOUR COUNTER
F.F.

CS 6 883



1002	M 4
1101	E 8
1102	E 7
1103	F 2
1104	G 2
1105	K 4
1106	M 4
1107	K 9
1108	M11
2001	M 2
2002	M 2
2003	N 2
2004	M 3
2005	M 3
2006	N 3
2007	G13
2008	G 5
2009	A 3
2010	G 7
2011	H 3
2012	I 20
2013	I 20
2014	L22
2015	L22
2016	L 2
2017	K 2
2018	J 6
2019	J 7
2020	M12
2021	M13
2023	I 11
2101	A 3
2102	B 8
2103	A12
2104	A 5
2105	A15
2106	A18
2107	B24
2108	H18
2109	C20
2110	G 7
2111	G13
2112	K20
2113	G21
2114	J21
2115	D 2
2117	J 9
3001	C13
3002	N 4
3004	J 5
3005	K 5
3006	K 5
3007	H 4
3008	H 4
3009	J 8
3010	J 6
3011	K 8
3012	K 8
3013	G 6
3014	G 7
3015	I 22
3016	H16
3017	H16
3018	H16
3019	H17
3020	J16
3021	J16
3022	J16
3023	J17
3028	M 4
3030	H 8
3031	M 7
3032	M 7
3033	M 8
3034	M 8
3035	H 9
3036	G10
3037	H10
3038	G10
3039	I 10
3040	H10
5001	L 2
5002	M 2
5003	M 2
5101	K 2
5102	M12
6001	J 7
6002	H 4
6003	M 4
6009	H 8
6010	G 9
7002	K 5
7003	J 8
7004	G 4
7005	M 8
7006	G 9
7007	G10
7008	I 10
7201	B 2
7202	B 7
7203	A12
7204	A 4
7205	A15
7206	A18
7207	B23
7208	H18
7209	C20
7210	G 5
7211	G12
7213	G21
7214	K21
7215	B20
7215	B21
7215	B17
7215	E 1
7217	J10
7217	K10
7217	L 9
7217	M 9

CONTROL MODULE S

(MOD. LEVEL 3)

LIST OF ELECTRICAL PARTS MODULE S

Eproms (programmed)
7202   4822 209 51256   TMS 27512 control

Batteries
1002   4822 138 10032   Battery 2.4 V

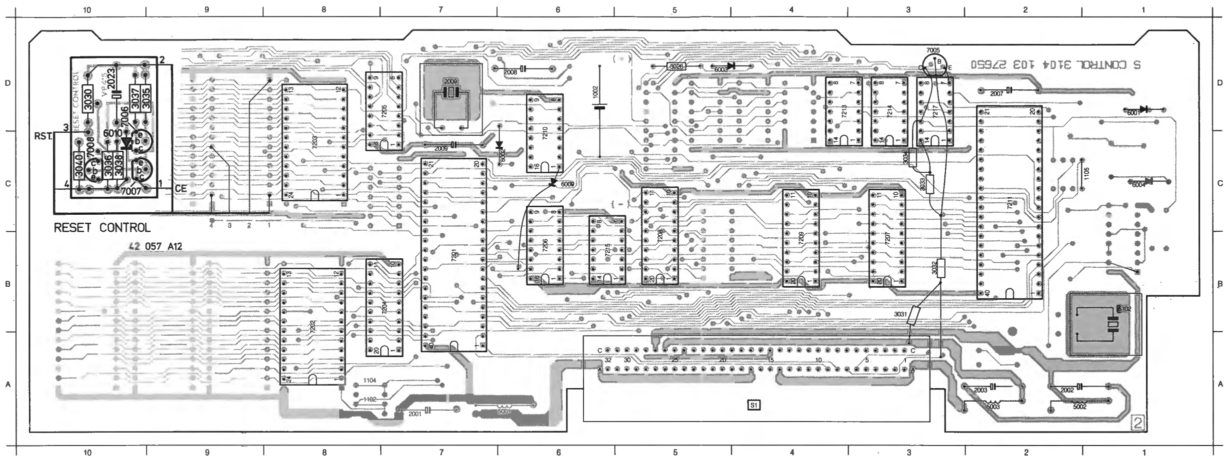
Crystals
5101   4822 242 70917   11.059 MHz
5102   4822 242 70668   4 MHz

Coils
5001   4822 158 10101   5.3 µH
5002   4822 158 10101   5.3 µH
5003   4822 158 10101   5.3 µH

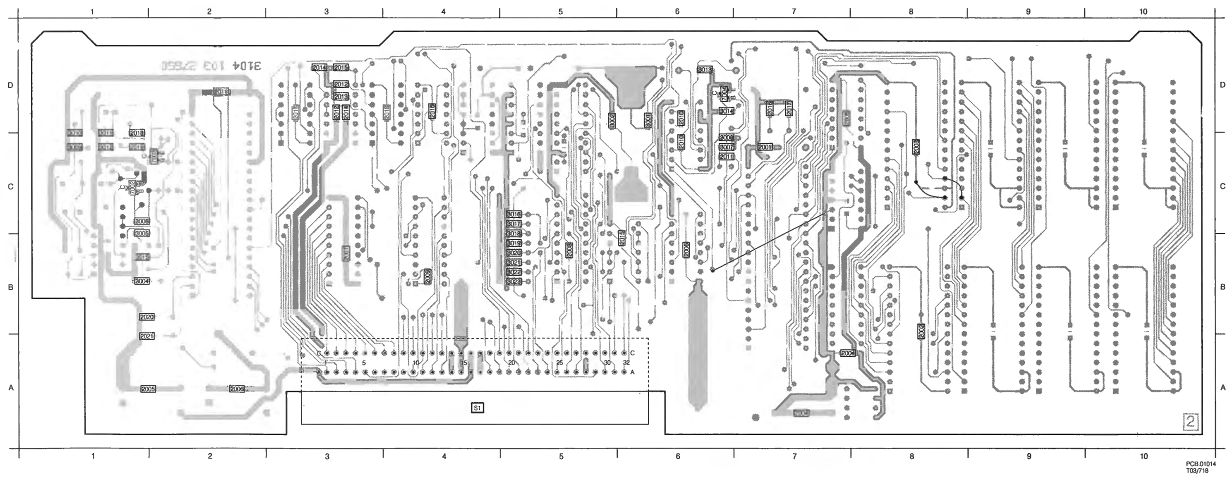
NFR25 Resistors
3028   4822 111 30483   1 Ω

2001	4822 124 22027	47 µF	25 V
2002	5322 124 21749	10 µF	63 V
2003	5322 124 21749	10 µF	63 V
2004	4822 122 31759	22 nF	
2005	4822 122 31759	22 nF	
2006	4822 122 31759	22 nF	
2007	4822 124 22027	47 µF	25 V
2008	4822 124 22029	2.2 µF	63 V
2009	4822 124 22027	47 µF	25 V
2010	4822 122 31759	22 nF	
2011	4822 122 31644	2.2 nF	
2012	4822 122 31966	27 pF	
2013	4822 122 31966	27 pF	
2014	4822 122 32976	470 pF	
2015	4822 122 32976	470 pF	
2016	4822 122 32975	33 pF	
2017	4822 122 32975	33 pF	
2018	4822 122 33009	270 nF	25 V
2019	4822 122 31644	2.2 nF	
2020	4822 122 32482	22 pF	
2021	4822 122 32482	22 pF	
2023	4822 124 22028	1 µF	63 V
2101	4822 122 31759	22 nF	
2102	4822 122 31759	22 nF	
2103	4822 122 31759	22 nF	
2104	4822 122 31759	22 nF	
2105	4822 122 31759	22 nF	
2106	4822 122 31759	22 nF	
2107	4822 122 31759	22 nF	
2108	4822 122 31759	22 nF	
2109	4822 122 31759	22 nF	
2110	4822 122 31759	22 nF	
2111	4822 122 31759	22 nF	
2112	4822 122 31759	22 nF	
2113	4822 122 31759	22 nF	
2114	4822 122 31759	22 nF	
2115	4822 122 31759	22 nF	
2116	4822 122 31759	22 nF	
2117	4822 122 31759	22 nF	

1002 D 6	1104 A 8	2001 A 7	2003 A 3	2008 D 7	2009 D 7	3031 B 3	3033 C 3	5001 A 7	5003 A 2	6001 D 1	6003 D 5	6009 C 6	7201 B 7	7203 C 8	7205 D 7	7207 B 3	7209 B 4	7211 C 2	7214 D 3	7217 D 3
1102 A 8	1105 C 1	2002 A 2	2007 D 2	2009 C 7	3028 D 5	3032 B 3	3034 C 3	5002 A 2	5102 B 1	6002 C 6	6004 C 1	7005 D 3	7202 A 8	7204 B 7	7206 B 6	7208 B 5	7210 C 6	7213 D 3	7215 B 6	



2001 C 7	2004 A 7	2005 C 7	2007 B 3	2010 C 6	2011 C 6	2013 D 3	2014 D 3	2016 D 4	2017 D 7	2020 B 2	3002 C 5	3006 C 1	3009 C 1	3012 C 1	3015 B 1	3018 B 5	3021 B 5	7002 C 1
2002 A 8	2004 A 7	2006 A 2	2008 B 5	2010 C 6	2012 D 3	2013 D 4	2015 D 3	2016 D 7	2018 C 1	2021 A 2	3004 B 1	3007 C 6	3010 C 1	3013 D 6	3016 C 5	3019 B 5	3022 B 5	7003 C 2
2003 C 8	2005 A 2	2006 B 6	2009 B 4	2011 D 2	2012 D 3	2014 D 3	2015 B 6	2017 D 3	2019 C 1	3001 C 6	3005 B 1	3008 C 6	3011 C 1	3014 D 6	3017 C 5	3020 B 5	3023 B 5	7004 D 6



SUPPLY MODULE [T]

(MOD LEVEL 1)

ADJUSTMENTS

Required
Test disc
Voltmeter

Adjustment conditions
Rotating disc

Adjustments

1) **R503** (DC Voltage)
   –Measure the DC voltage on 3T2 (+5)
   –Adjust R503 for 5.2V (±0.1V)

LIST OF ELECTRICAL PARTS MODULE T

Fuses

F911	4822 253 30024	1.6 A
F912	4822 253 30024	1.6 A
F913	4822 253 10048	3.15 A

Circuits

D501	5322 209 82349	Hybride circuit SMPS

Diodes

V001	4822 130 50438	Rectifier KBU8–K

Transformers

T101	5322 146 40322	aux trafo
T201	5322 142 60363	impuls trafo
T401	4822 142 70056	current trafo
T901	5322 146 30531	power trafo

Coils

L001	4822 157 52981	350 µH
L002	4822 158 30208	Mains choke
L701	4822 157 52979	Triple choke

Potentiometers

R402	4822 101 10793	5 kΩ
R503	4822 101 10792	1 kΩ

NTC Resistors

R001	5322 116 40077	7 Ω

PTC Resistors

R801	4822 116 40032	2.3 Ω – 5 Ω

Wire wound Resistors

R201	4822 112 41107	1 kΩ

NFR25 Resistors

R101	4822 111 30544	220 Ω
R202	4822 111 30526	47 Ω
R301	4822 111 30499	4.7 Ω
R701	4822 111 30526	47 Ω
R702	4822 111 30526	47 Ω
R706	4822 111 30526	47 Ω

VR25 Resistors

R901	5322 116 64132	1 MΩ

PR37 Resistors

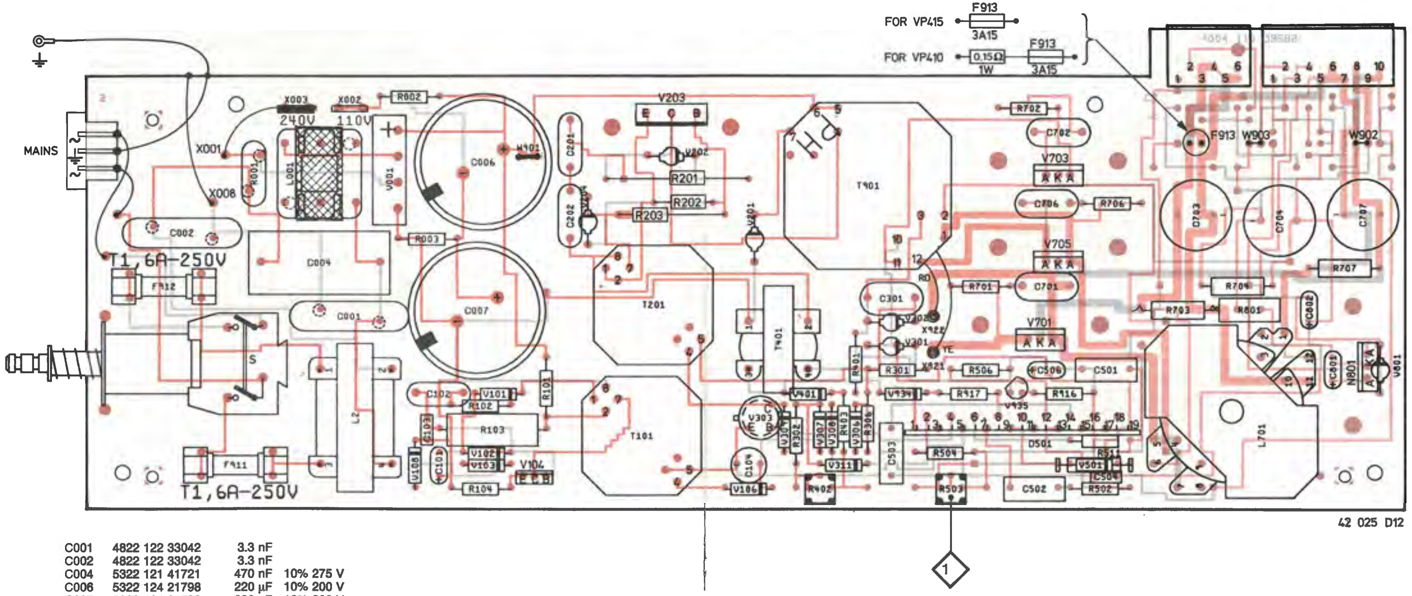
R703	5322 116 55063	39 Ω
R704	5322 116 54909	1 kΩ
R707	5322 116 54909	1 kΩ

PR52 Resistors

R203	5322 116 51093	15 Ω

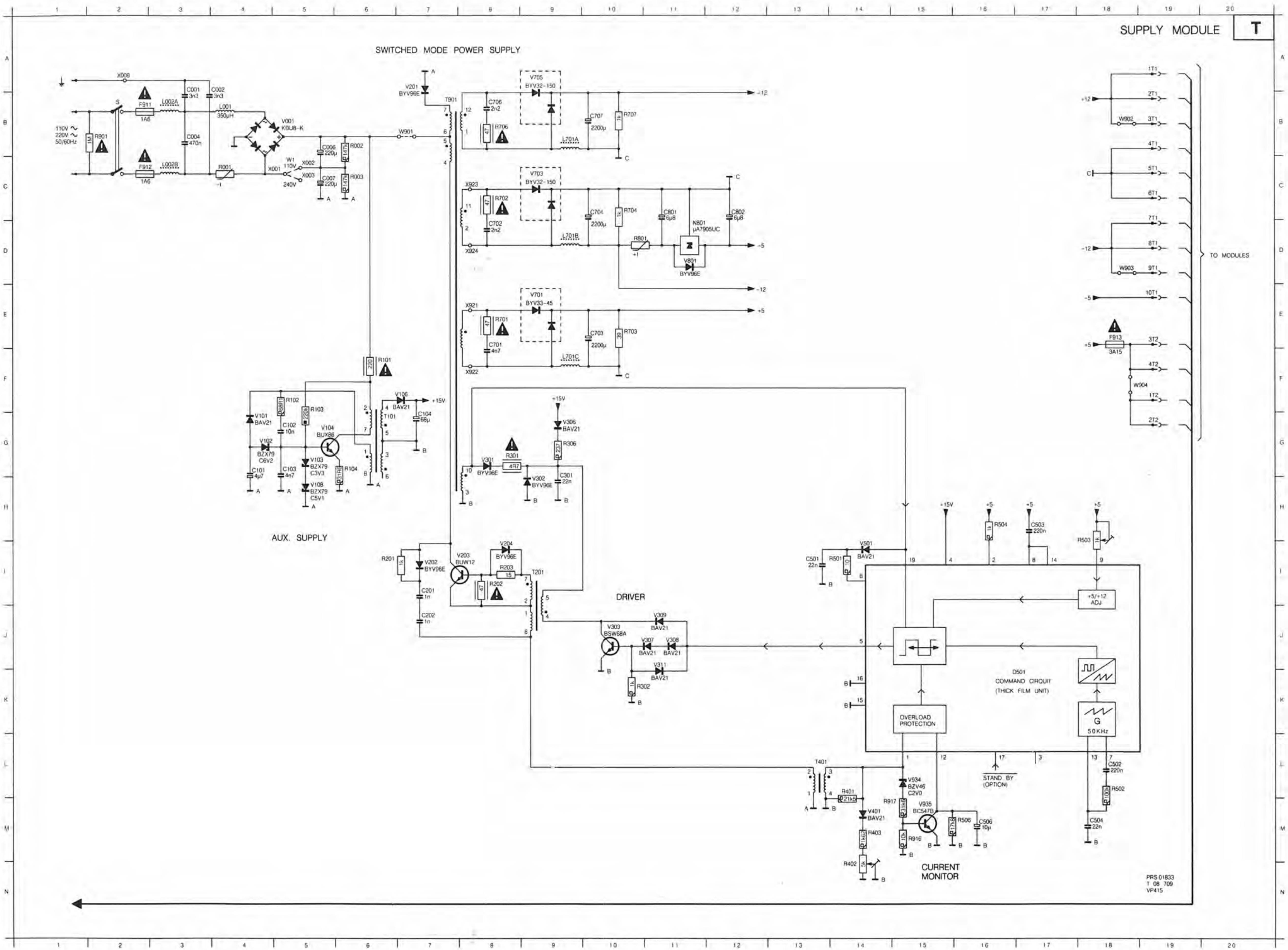
VR68 Resistors

R103	5322 116 53075	220 kΩ

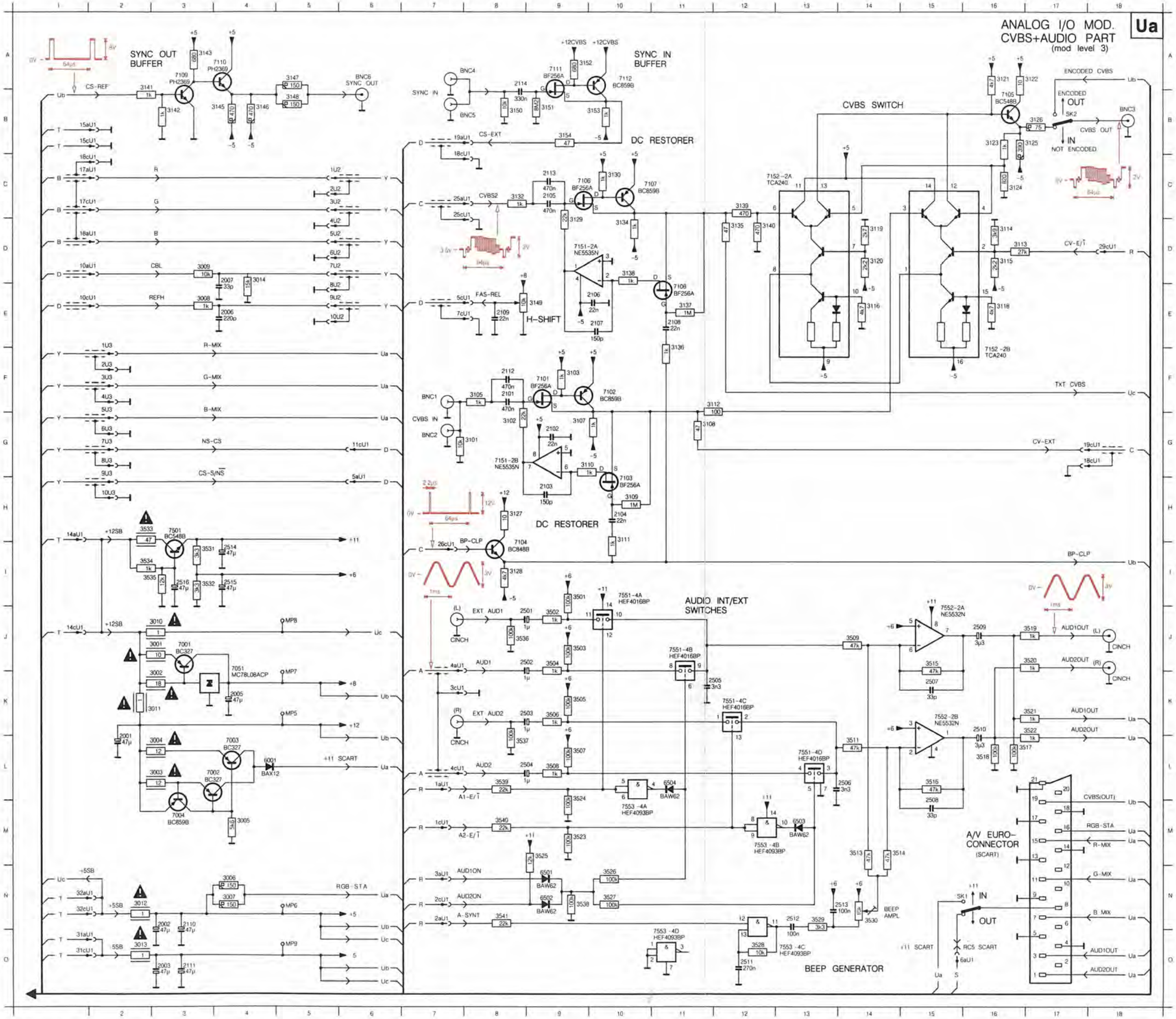


C001	4822 122 33042	3.3 nF	
C002	4822 122 33042	3.3 nF	
C004	5322 121 41721	470 nF	10% 275 V
C006	5322 124 21798	220 µF	10% 200 V
C007	5322 124 21798	220 µF	10% 200 V
C101	4822 124 10367	4.7 µF	25 V
C102	4822 121 40483	10 nF	10% 400 V
C103	4822 122 31125	4.7 nF	100 V
C104	4822 124 40744	68 µF	40 V
C201	5322 121 44286	1 nF	10% 630 V
C202	5322 121 44286	1 nF	10% 630 V
C301	4822 121 40516	22 nF	10% 250 V
C501	5322 121 40308	22 nF	10% 400 V
C502	4822 121 40232	220 nF	10% 100 V
C503	4822 121 40232	220 nF	10% 100 V
C504	4822 122 30103	22 nF	63 V
C506	4822 124 21314	10 µF	16 V
C701	4822 121 40337	4.7 nF	10% 630 V
C702	4822 121 40338	2.2 nF	10% 630 V
C703	4822 124 40723	2.2 mF	16 V
C704	4822 124 40723	2.2 mF	16 V
C706	4822 121 40338	2.2 nF	10% 630 V
C707	4822 124 40723	2.2 mF	16 V
C801	5322 124 14081	6.8 µF	25 V
C802	5322 124 14081	6.8 µF	25 V

C001	A 3	C007	C 5	C104	G 7	C501	I 14	C506	M16	C704	C10	C802	C12	F913	E18	L701A	B 9	R001	C 4	R102	F 5	R202	I 8	R306	G 9	R501	I 14	R506	M16	R704	C10	R901	B 2	T101	G 6	V001	B 5	V104	G 5	V202	I 7	V302	H 9	V308	J11	V501	I 15	V801	D11	W901	B 7
C002	A 4	C101	G 4	C201	I 7	C502	L18	C701	E 8	C706	B 8	D501	J17	L001	B 4	L701B	D 9	R002	B 6	R103	F 5	R203	I 8	R401	L14	R502	L19	R701	E 8	R706	B 8	R916	M15	T201	I 9	V101	G 4	V106	F 7	V203	I 8	V303	J10	V309	J11	V701	E 9	V934	L15	W902	B18
C004	B 3	C102	G 5	C202	J 7	C503	H17	C702	D 8	C707	B10	F911	B 2	L002A	B 3	L701C	F 9	R003	C 6	R104	G 6	R301	G 8	R402	N14	R503	H18	R702	C 8	R707	B10	R917	M15	T401	L13	V102	G 4	V108	H 5	V204	I 8	V306	G 9	V311	J11	V703	C 9	V935	M15	W903	D18
C006	B 5	C103	G 5	C301	G 9	C504	M18	C703	E10	C801	C11	F912	C 2	L002B	C 3	N801	D11	R101	F 6	R201	I 6	R302	K11	R403	M14	R504	H17	R703	E10	R801	D10	S	B 2	T901	B 7	V103	G 5	V201	A 7	V301	G 8	V307	J11	V401	M14	V705	A 9	WI	C 5	W904	F19



CS 6 885



2001	L 2
2002	N 3
2003	O 3
2005	K 4
2006	E 4
2007	D 4
2101	F 8
2102	G 9
2103	H 9
2104	H10
2105	C 9
2106	E10
2107	E10
2108	E11
2109	E 8
2110	N 3
2111	O 3
2112	F 8
2113	C 9
2114	A 8
2501	J 9
2502	J 9
2503	K 9
2504	L 9
2505	K12
2506	L14
2507	K15
2508	L15
2509	J16
2510	K16
2511	O12
2512	N13
2513	N14
2514	I 4
2515	I 4
2516	I 3
3001	J 3
3002	K 3
3003	L 3
3004	L 3
3005	M 4
3006	N 4
3007	N 4
3008	E 3
3009	D 3
3010	J 3
3011	K 3
3012	N 2
3013	O 2
3014	D 4
3101	G 8
3102	G 8
3103	F 9
3105	F 8
3107	G 9
3108	G11
3109	H10
3110	G 9
3111	H10
3112	F12
3113	D16
3114	D16
3115	D16
3116	E14
3118	E16
3119	D14
3120	D14
3121	A16
3122	A17
3123	B16
3124	C16
3125	B17
3126	B17
3127	H 8
3128	I 8
3129	D 9
3130	C10
3132	C 8
3134	D10
3135	D12
3136	E11
3137	E11
3138	D10
3139	C12
3140	D12
3141	A 2
3142	B 3
3143	A 3
3145	B 4
3146	B 4
3147	A 5
3148	B 5
3149	E 9
3150	B 8
3151	B 9
3152	A10
3153	B10
3154	B 9
3501	I 9
3502	J 9
3503	J 9
3504	J 9
3505	K 9
3506	K 9
3507	L 9
3508	L 9
3509	J14
3511	L14
3513	M14
3514	M15
3515	J15
3516	L15
3517	L17
3518	L16
3519	J17
3520	J17
3521	K17
3522	K17
3523	M 9
3524	L 9
3525	M 9
3526	N10
3527	N10
3528	O12
3529	N13
3530	N14
3531	I 3
3532	I 3
3533	H 2
3534	I 2
3535	I 3
3536	J 8
3537	L 8
3538	N 9
3539	L 8
3540	M 8
3541	N 8
6001	L 4
6501	N 9
6502	N 9
6503	M13
6504	L11
7001	J 3
7002	L 4
7003	L 4
7004	M 3
7051	J 4
7101	F 9
7102	F10
7103	H10
7104	I 8
7105	B16
7106	C 9
7107	C10
7108	E11
7109	A 3
7110	A 4
7111	A 9
7112	A10
7151	D 9
7151	G 8
7152	C13
7152	F16
7501	H 3
7551	I10
7551	J11
7551	K12
7551	L13
7552	J15
7552	K15
7553	M10
7553	O11
7553	O13
7553	M12
BNC1	F 7
BNC2	G 7
BNC3	B18
BNC4	A 8
BNC5	B 8
BNC6	A 6
SK1	N16
SK2	B17

PRS 01088
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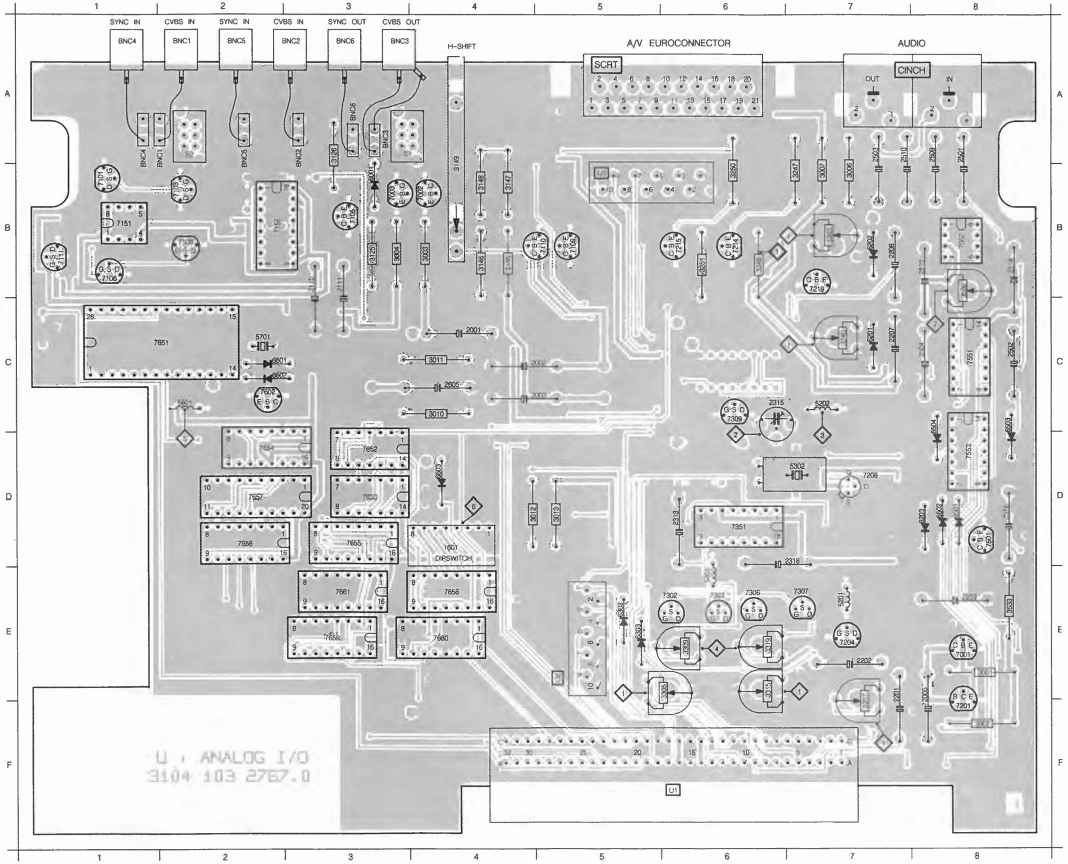
VP415

ANALOG I/O MODULE U

(MOD. LEVEL 3)

2001 C 4	2201 E 7	2315 C 6	2509 A 8	3001 E 8	3010 C 4	3145 B 4	3240 C 7	3305 E 6	5201 E 7
2002 C 5	2202 E 7	2318 D 7	2510 A 7	3002 F 8	3011 C 4	3146 B 4	3247 B 7	3309 E 6	5202 C 7
2003 C 5	2203 E 8	2501 A 8	2514 B 8	3003 B 4	3012 D 4	3147 B 4	3248 B 6	3315 E 6	5301 E 6
2005 E 8	2207 C 7	2502 C 8	2515 B 8	3004 B 3	3013 D 5	3148 B 4	3250 B 6	3319 E 6	5302 D 7
2110 B 3	2208 B 7	2503 A 7	2516 D 8	3006 B 7	3125 B 3	3149 A 4	3251 B 6	3530 B 8	5601 C 2
2111 B 3	2313 D 6	2504 C 8	2605 C 4	3007 B 7	3126 A 3	3207 E 7	3263 B 7	3533 E 8	5701 C 2

6001 B 3	6501 D 8	6603 D 4	7105 B 3	7151 B 1	7215 B 6	7309 C 6	7602 C 2	7656 E 4	BNC1 A 2
6201 C 7	6502 D 8	7001 E 8	7106 B 1	7152 B 2	7219 B 7	7351 D 6	7651 C 2	7657 D 2	BNC2 A 3
6202 B 7	6503 C 8	7002 B 4	7108 B 2	7201 F 8	7302 E 6	7501 D 8	7652 D 3	7658 D 2	BNC3 A 3
6203 D 8	6504 C 8	7003 B 3	7109 B 5	7204 E 7	7303 E 6	7551 C 8	7653 D 3	7659 E 3	BNC4 A 1
6302 E 5	6601 C 2	7101 B 1	7110 B 5	7208 D 7	7306 E 6	7552 B 8	7654 D 2	7660 E 4	BNC5 A 2
6303 E 5	6602 C 2	7103 B 2	7111 B 1	7214 B 6	7307 E 7	7553 D 8	7655 D 3	7661 E 3	BNC6 A 3



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2101 A 1	2302 E 6	2506 C 8	2612 C 2	3008 E 5	3116 B 2	3137 B 2	3205 E 8	3222 D 7	3238 C 7
2102 B 1	2304 F 6	2507 B 8	2613 C 3	3009 E 5	3118 B 2	3138 B 2	3206 F 7	3223 D 7	3239 B 7
2103 B 1	2305 E 6	2508 B 8	2614 D 3	3014 E 5	3119 B 2	3139 B 2	3208 E 8	3224 D 7	3241 C 6
2104 B 2	2307 D 6	2511 C 8	2615 C 2	3101 A 2	3120 B 3	3140 B 2	3209 E 8	3225 D 7	3242 B 6
2105 B 2	2308 D 6	2512 D 8	2616 D 3	3102 B 1	3121 B 3	3141 B 5	3210 E 7	3226 D 7	3243 B 7
2106 B 1	2309 D 6	2513 B 8	2617 D 3	3103 B 1	3122 B 3	3142 B 5	3211 E 7	3227 D 7	3244 B 6
2107 B 1	2310 D 6	2601 C 1	2618 D 3	3105 A 1	3123 B 2	3143 B 5	3212 E 8	3228 D 7	3245 B 6
2108 B 2	2311 D 6	2602 C 1	2619 E 3	3107 B 2	3124 B 2	3150 A 1	3213 E 7	3229 D 7	3246 B 6
2109 B 4	2312 D 6	2603 C 2	2620 E 4	3108 B 2	3127 D 5	3151 A 1	3214 E 7	3230 D 7	3249 B 6
2112 B 1	2314 D 6	2604 D 2	2621 D 3	3109 B 2	3128 D 5	3152 B 1	3215 E 7	3231 D 7	3252 D 7
2113 B 2	2316 C 6	2606 C 2	2622 D 2	3110 B 2	3129 B 1	3153 B 1	3216 E 7	3232 C 7	3253 D 7
2114 A 1	2319 D 6	2607 C 1	2623 E 3	3111 B 2	3130 B 1	3154 B 1	3217 D 7	3233 E 6	3254 D 8
2204 E 7	2323 C 6	2608 C 1	2624 E 4	3112 B 2	3132 B 2	3201 D 7	3218 D 7	3234 E 7	3255 D 8
2205 E 7	2324 C 6	2609 C 1	2625 C 2	3113 B 3	3134 B 2	3202 E 8	3219 D 7	3235 D 7	3256 C 7

3257 D 8	3311 E 7	3340 E 7	3514 B 8	3531 B 8	3607 C 2	3623 D 2	3639 E 3	7210 D 6	7311 F 7
3258 C 7	3312 F 6	3341 E 6	3515 B 8	3532 B 8	3608 C 2	3624 D 3	3640 C 2	7211 C 7	7601 C 1
3259 C 6	3313 E 7	3342 E 6	3516 B 8	3534 E 8	3609 C 3	3625 D 3	3642 D 2	7212 C 7	7603 D 4
3260 B 7	3314 E 7	3343 C 5	3517 A 7	3535 D 8	3610 C 3	3626 D 3	3643 E 3	7213 B 6	7604 F 4
3261 B 7	3318 E 6	3344 F 6	3518 A 8	3536 A 8	3611 D 3	3627 D 3	7004 B 4	7216 C 5	7605 E 4
3262 B 7	3320 E 7	3501 C 8	3519 A 8	3537 A 8	3612 D 2	3628 E 4	7102 A 1	7217 D 7	
3264 B 7	3321 E 5	3502 C 8	3520 A 7	3538 D 8	3613 D 2	3629 E 4	7104 D 5	7218 C 7	
3265 D 7	3322 D 6	3503 C 8	3521 A 5	3539 F 8	3614 C 3	3630 E 4	7107 B 1	7220 B 7	
3301 E 6	3323 D 6	3504 C 8	3522 A 5	3540 F 8	3615 C 3	3631 E 4	7112 B 1	7221 D 7	
3302 E 6	3324 D 6	3505 C 8	3523 D 8	3541 F 8	3616 C 3	3632 D 2	7201 E 7	7222 C 7	
3303 E 6	3325 D 6	3506 C 8	3524 D 8	3601 B 1	3617 D 4	3633 D 2	7202 E 7	7223 D 7	
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3306 E 5	3330 C 6	3508 C 8	3526 D 8	3603 B 1	3619 D 4	3635 F 4	7205 D 7	7304 E 6	
3307 E 6	3331 C 6	3509 B 8	3527 D 8	3604 B 1	3620 D 4	3636 E 4	7206 D 7	7305 E 7	
3308 E 6	3338 D 6	3511 B 8	3528 C 8	3605 C 1	3621 D 2	3637 E 4	7207 D 7	7308 E 7	
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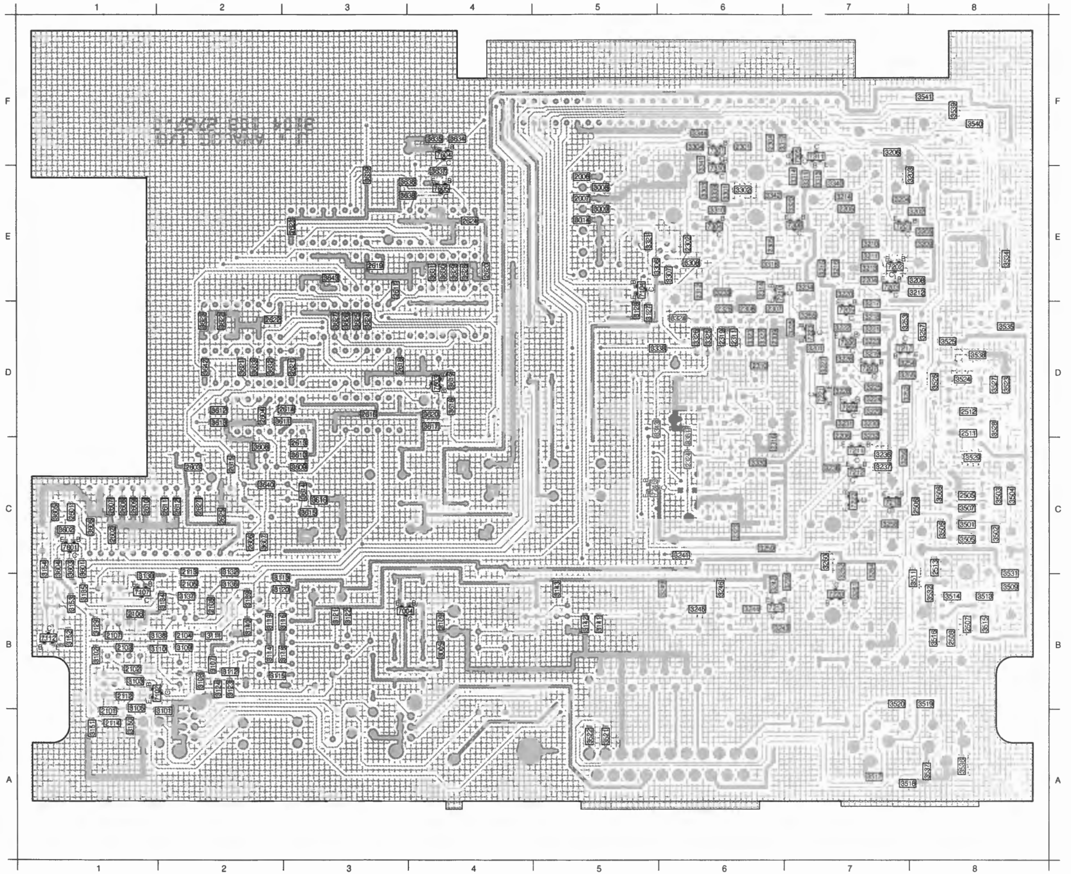

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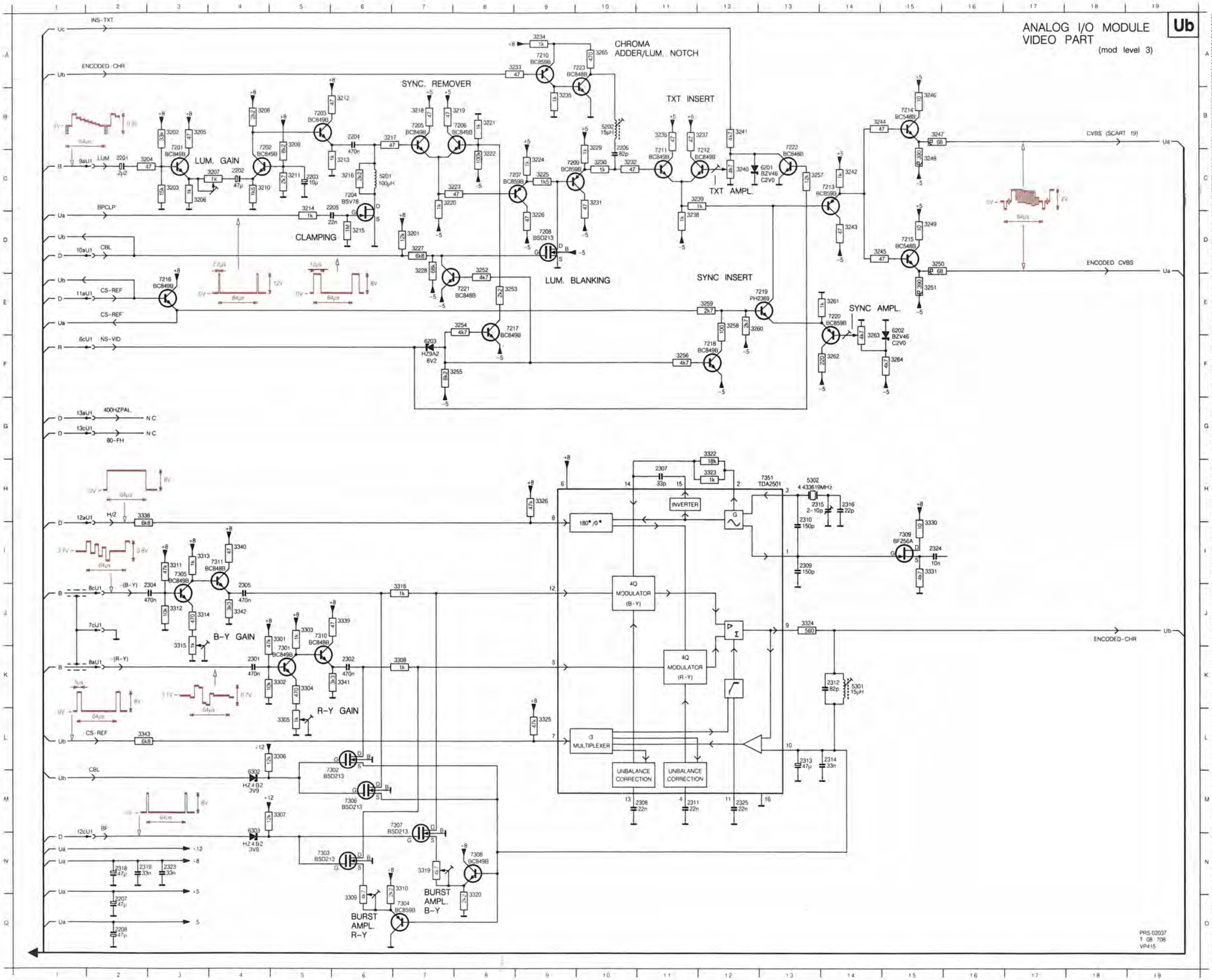

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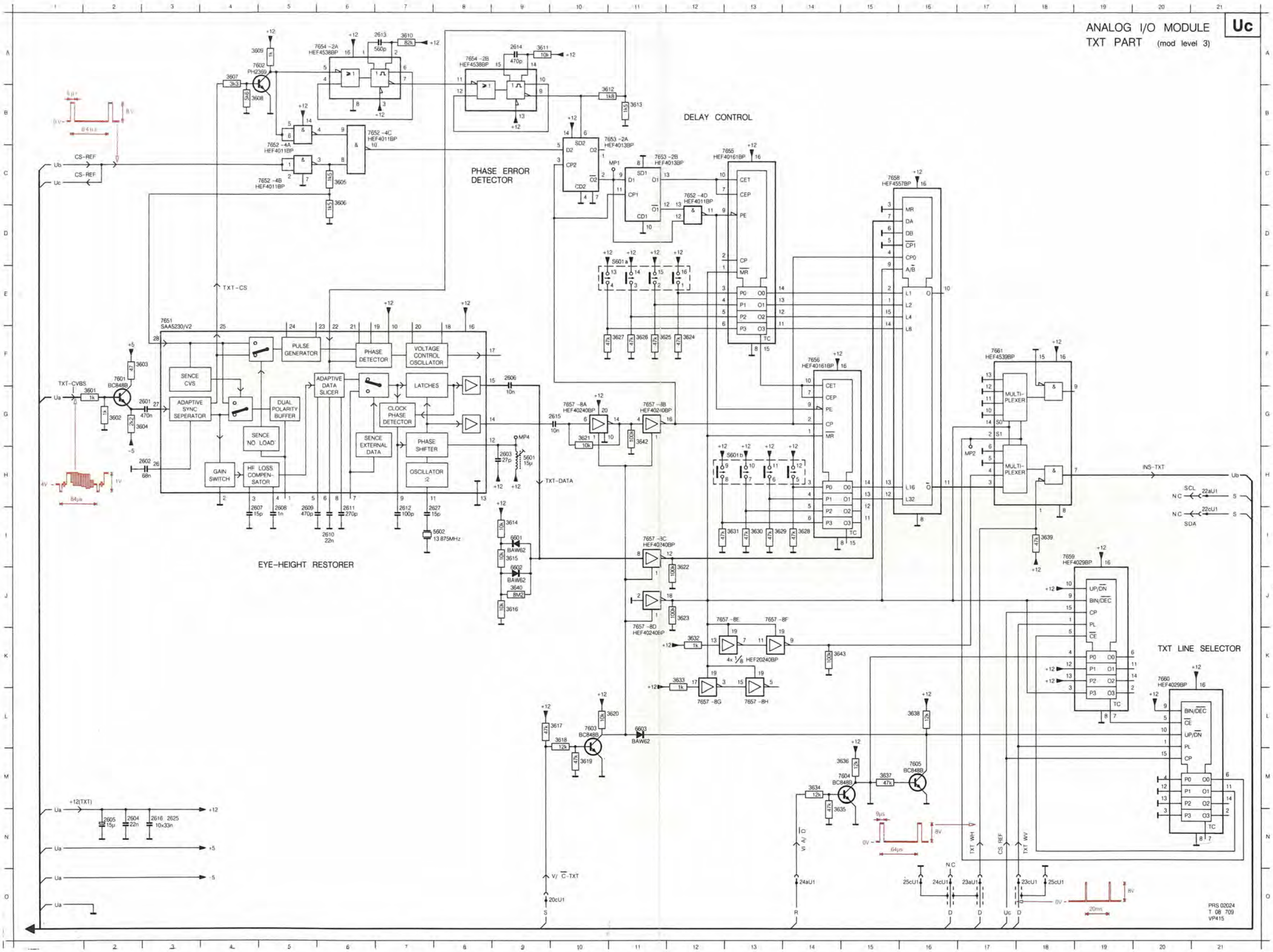
2202	C 4	7219	E13
2203	C 5	7220	E14
2204	B 6	7221	E 8
2205	C 6	7222	B13
2206	B10	7223	A10
2207	O 2	7301	K 5
2208	O 2	7302	L 6
2301	K 4	7303	N 5
2302	K 6	7304	O 7
2304	J 3	7305	I 3
2305	J 4	7306	M 6
2307	H11	7307	M 7
2308	M11	7308	N 8
2309	I 13	7309	I 15
2310	H13	7310	J 5
2311	M11	7311	I 4
2312	K14	7351	H13
2313	L13		
2314	L14		
2315	H14		
2316	H14		
2318	N 2		
2319	N 3		
2323	N 3		
2324	I 15		
2325	M12		
3201	D 7		
3202	B 3		
3203	C 3		
3204	C 2		
3205	B 3		
3206	C 3		
3207	C 4		
3208	B 4		
3209	B 5		
3210	C 4		
3211	C 5		
3212	B 6		
3213	C 6		
3214	C 5		
3215	D 6		
3216	C 6		
3217	B 6		
3218	B 7		
3219	B 8		
3220	C 7		
3221	B 8		
3222	C 8		
3223	C 8		
3224	C 9		
3225	C 9		
3226	D 9		
3227	D 7		
3228	D 7		
3229	B10		
3230	C10		
3231	C10		
3232	C10		
3233	A 9		
3234	A 9		
3235	B 9		
3236	B11		
3237	B12		
3238	D11		
3239	C12		
3240	C12		
3241	B12		
3242	C14		
3243	D14		
3244	B14		
3245	D14		
3246	B15		
3247	B15		
3248	C15		
3249	D15		
3250	D15		
3251	E15		
3253	E 8		
3254	E 8		
3255	F 8		
3256	F11		
3257	C14		
3258	E12		
3259	E12		
3260	E13		
3261	E14		
3262	F14		
3263	E14		
3264	F15		
3265	A10		
3301	J 5		
3302	K 5		
3303	J 5		
3304	K 5		
3305	L 5		
3306	L 5		
3307	M 5		
3308	K 7		
3309	O 6		
3310	N 7		
3311	I 3		
3312	J 3		
3313	I 3		
3314	J 3		
3315	J 3		
3318	J 7		
3319	N 7		
3320	N 8		
3322	G12		
3323	H12		
3324	J13		
3325	L 9		
3326	H 9		
3330	I 15		
3331	I 15		
3338	H 2		
3339	J 6		
3340	I 4		
3341	K 6		
3342	J 4		
3343	L 2		
5201	C 6		
5202	B10		
5301	K14		
5302	H13		
6201	C13		
6202	E15		
6203	F 7		
6302	M 4		
6303	M 4		
7201	B 3		
7202	B 4		
7203	B 5		
7204	C 6		
7205	B 7		
7206	B 8		
7207	C 9		
7208	D 9		
7209	C 9		
7210	A 9		
7211	C11		
7212	C12		
7213	C14		
7214	B15		
7215	D15		
7216	E 3		
7217	E 8		

ANALOG I/O MODULE TXT PART (mod level 3)

Uc



2601	G 3
2602	H 3
2603	H 9
2604	N 2
2605	N 2
2606	F 9
2607	I 5
2608	I 5
2609	I 5
2610	I 6
2611	I 6
2612	I 7
2613	A 7
2614	A 9
2615	G10
2627	I 8
3601	G 2
3602	G 2
3603	F 3
3604	G 3
3605	C 6
3606	C 6
3607	A 4
3608	B 5
3609	A 5
3610	A 7
3611	A 9
3612	B11
3613	B11
3614	I 9
3615	I 9
3616	J 9
3617	L10
3618	L10
3619	M10
3620	L11
3621	G10
3622	I 12
3623	J12
3624	F12
3625	F12
3626	F11
3627	F11
3628	I 14
3629	I 14
3630	I 13
3631	I 13
3632	K12
3633	K12
3634	M14
3635	N15
3636	M15
3637	M15
3638	L16
3639	I 18
3640	J 9
3642	G11
3643	K15
5601	H 9
5602	I 8
6601	I 9
6602	J 9
6603	L11
7601	F 2
7602	A 5
7603	L10
7604	M15
7605	M16
7651	E 3
7652	B 5
7652	B 7
7652	C 5
7652	C12
7653	B11
7653	C11
7654	A 6
7654	A 8
7655	C13
7656	F14
7657	J13
7657	I 11
7657	G10
7657	G11
7657	J11
7657	J13
7657	L12
7657	L13
7658	C15
7659	I 18
7660	K20
7661	F17
2615 2626	N3

ANALOG I/O MODULE U

(MOD. LEVEL 3)

ADJUSTMENTS

Required
Test disc
Scope

Adjustment conditions
Load test disc.
Still picture, picture no. 6200 (colour bar EBU test signal).
Disc drive may not be locked to an external video source.

Adjustments

1) **R3263, R3207, R3240, R3315, R3305** (CVBS amplitudes)
   - Measure the CVBS OUT signal (ENCODED) on BNC3 (linefrequent) with the scope (see fig. U1). Terminate the signal with 75 Ω.

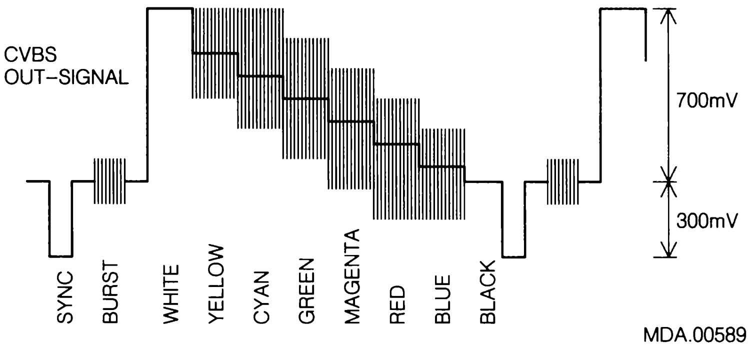
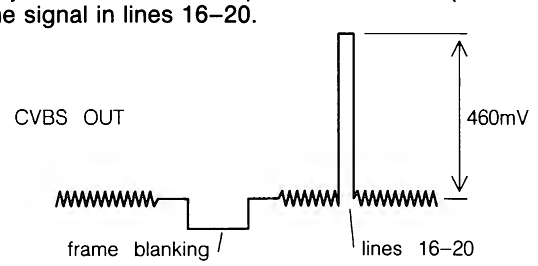


Fig. U1

- Adjust R3263 for a sync-amplitude of 300 mV relative to black level.
- Adjust R3207 for a white amplitude of 700 mV relative to black level.
- Adjust R3315 until the upper side of the chroma signal during the yellow bar lies at the same level as the white signal (700 mV).
- Adjust R3305 until the upper side of the chroma signal during the cyan bar lies at the same level as the white signal.
- Search for picture number 8200 (black) and switch off the index.
- Measure the CVBS OUT signal, frame frequent and display the lines 16–20 of the video signal. The VITS- and 24 bit code are displayed as TXT info (see Fig. U2).
- Adjust R3240 for an amplitude of 460 mV (±20 mV) of the signal in lines 16–20.



TXT AMPLITUDE

Fig. U2

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2) **C2315** (chroma subcarrier)
   - Measure with the scope (channel A) the CVBS OUT-signal on BNC3 (ENCODED).
   - Measure with the scope (channel B) the CVBS signal on E-TS7105 (NOT ENCODED).
   - Switch the scope to A+B, adding the 2 signals.
   - Adjust C2315 for minimum amplitude variations in the chroma signal.

3) **L5202** (chroma notch)
   - Measure the CVBS OUT signal (ENCODED) on BNC3 with the scope (line-frequent). Terminate tl signal with 75 Ω.
   - Adjust L5202 for maximum amplitude of the chroma signal.

4) **R3309, R3319** (burst amplitude)
   - Switch the drive into the STAND BY position.
   - Measure the CVBS OUT signal (ENCODED) on BNC3 with the scope (line frequent).Terminate the signal with 75 Ω.
   - Short circuit pins 10 and 12 of IC7351.
   - Adjust R3309 for a burst amplitude of 210 mV (±10 mV).
   - Remove short circuiting of pins 10 and 12.
   - Short circuit pins 5 and 12 of IC7351.
   - Adjust R3319 for a burst amplitude of 210 mV (±10 mV).
   - Remove short circuit of pins 5 and 12. (The burst amplitude will increase to approx 300 mV).

LIST OF ELECTRICAL PARTS MODULE U

Crystals

5302	4822 242 70323	4.433619 MHz
5602	4822 242 71417	13.875 MHz

Coils

5201	4822 156 21324	100 µH
5202	4822 156 10996	15 µH
5301	4822 156 10996	15 µH
5601	4822 156 10996	15 µH

Potentiometers

3149	4822 101 90063	10 kΩ
3207	4822 100 20151	1 kΩ
3240	5322 101 10691	4.7 kΩ
3263	5322 101 10691	4.7 kΩ
3305	4822 100 20151	1 kΩ
3309	5322 101 10691	4.7 kΩ
3315	4822 100 20151	1 kΩ
3319	5322 101 10691	4.7 kΩ
3530	5322 101 10627	10 kΩ

Fuse Resistors

3533	4822 111 30831	47 Ω

NFR25 Resistors

3001	4822 111 30508	10 Ω
3002	4822 111 30515	18 Ω
3003	4822 111 30511	12 Ω
3004	4822 111 30511	12 Ω
3010	4822 111 30483	1 Ω
3011	4822 111 30483	1 Ω
3012	4822 111 30483	1 Ω
3013	4822 111 30483	1 Ω

Trim Capacitors

2315	4822 125 50062	10 pF

5) **L5601** (Eye–height restorer)
- Measure the AC signal on pin 12–IC7651 (=MP4). Use a FET probe 1:10 or a probe with a capacitance < 3 pF
- Adjust L5601 for maximum amplitude of the AC signal.

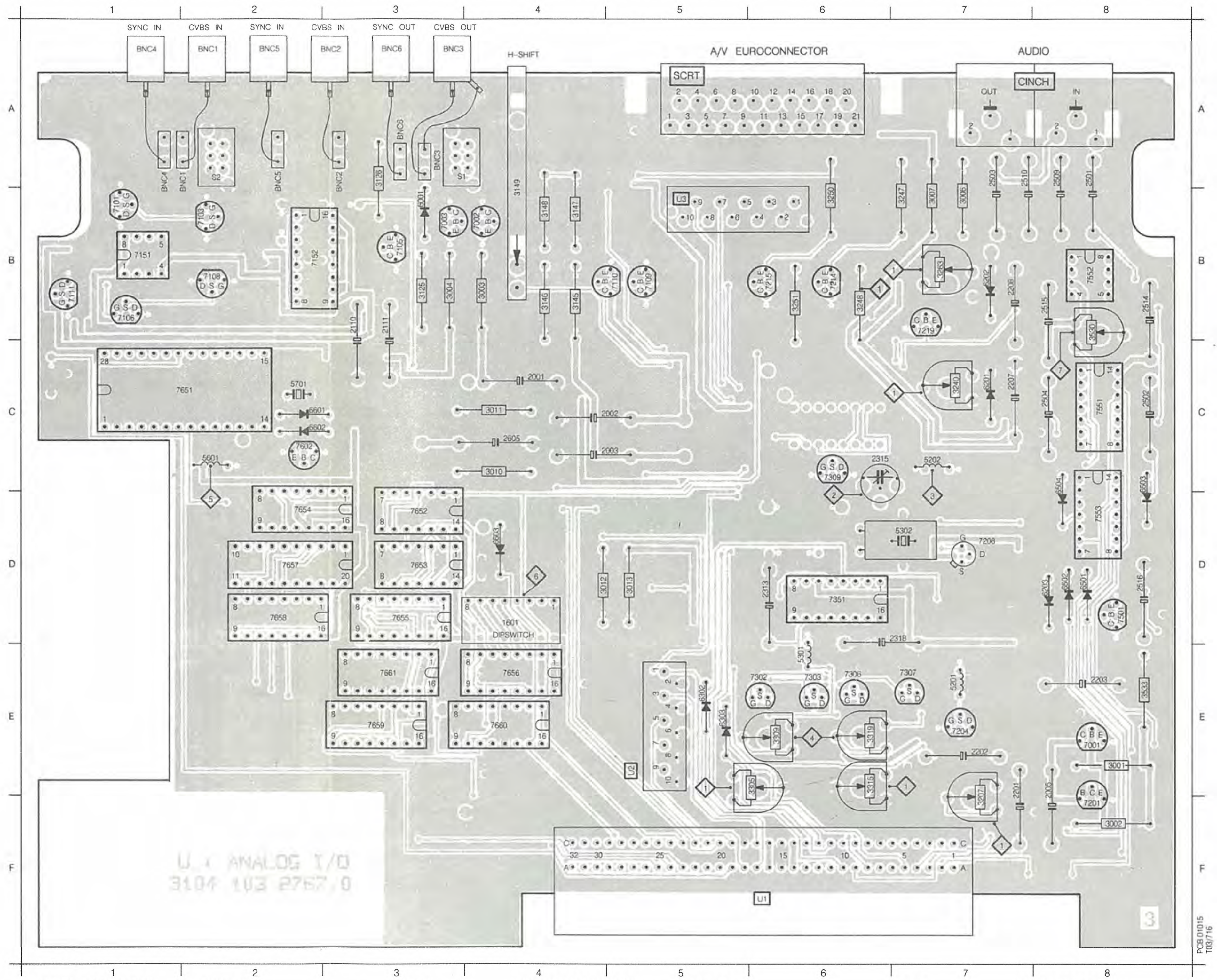
6) **S601** (Delay control)
- Switch S601 to be adjusted for a delay of approx 130 nsec,that means pins 1–16 of S601 interconnected (LSB bit P0=1), see diagram Uc.

7) **R3530** (Beep amplitude)
- Interconnect pins 12 and 14 of IC 7553.
- Measure the BEEP signal on cinch output AUD-1OUT and adjust R3530 until the beep signal is 300 mVpp ± 50 mV.

Adjustment when item replaced:

replaced	**adjust**
IC7351	R3305,R3315
RGB module	R3305,R3315

2001 C 4	2201 E 7	2315 C 6	2509 A 8	3001 E 8	3010 C 4	3145 B 4	3240 C 7	3305 E 6	5201 E 7	6001 B 3	6501 D 8	6603 D 4	7105 B 3	7151 B 1	7215 B 6	7309 C 6	7602 C 2	7656 E 4	BNC1 A 2
2002 C 5	2202 E 7	2318 D 7	2510 A 7	3002 F 8	3011 C 4	3146 B 4	3247 B 7	3309 E 6	5202 C 7	6201 C 7	6502 D 8	7001 E 8	7106 B 1	7152 B 2	7219 B 7	7351 D 6	7651 C 2	7657 D 2	BNC2 A 3
2003 C 5	2203 E 8	2501 A 8	2514 B 8	3003 B 4	3012 D 4	3147 B 4	3248 B 6	3315 E 6	5301 E 6	6202 B 7	6503 C 8	7002 B 4	7108 B 2	7201 F 8	7302 E 6	7501 D 8	7652 D 3	7658 D 2	BNC3 A 3
2005 E 8	2207 C 7	2502 C 8	2515 B 8	3004 B 3	3013 D 5	3148 B 4	3250 B 6	3319 E 6	5302 D 7	6203 D 8	6504 C 8	7003 B 3	7109 B 5	7204 E 7	7303 E 6	7551 C 8	7653 D 3	7659 E 3	BNC4 A 1
2110 B 3	2208 B 7	2503 A 7	2516 D 8	3006 B 7	3125 B 3	3149 A 4	3251 B 6	3530 B 8	5601 C 2	6302 E 5	6601 C 2	7101 B 1	7110 B 5	7208 D 7	7306 E 6	7552 B 8	7654 D 2	7660 E 4	BNC5 A 2
2111 B 3	2313 D 6	2504 C 8	2605 C 4	3007 B 7	3126 A 3	3207 E 7	3263 B 7	3533 E 8	5701 C 2	6303 E 5	6602 C 2	7103 B 2	7111 B 1	7214 B 6	7307 E 7	7553 D 8	7655 D 3	7661 E 3	BNC6 A 3



2001	4822 124 22027	47 µF	25 V
2002	4822 124 22027	47 µF	25 V
2003	4822 124 22027	47 µF	25 V
2005	4822 124 22027	47 µF	25 V
2006	4822 122 31965	220 pF	
2007	4822 122 32975	33 pF	
2101	4822 122 33011	470 nF	16 V
2102	4822 122 31759	22 nF	
2103	4822 122 31767	150 pF	
2104	4822 122 31759	22 nF	
2105	4822 122 33011	470 nF	16 V
2106	4822 122 31759	22 nF	
2107	4822 122 31767	150 pF	
2108	4822 122 31759	22 nF	
2109	4822 122 31759	22 nF	
2110	4822 124 22027	47 µF	25 V
2111	4822 124 22027	47 µF	25 V
2112	4822 122 33011	470 nF	16 V
2113	4822 122 33011	470 nF	16 V
2114	4822 122 33007	330 nF	25 V
2201	4822 124 22029	2.2 µF	63 V
2202	4822 124 22027	47 µF	25 V
2203	5322 124 21749	10 µF	63 V
2204	4822 122 33011	470 nF	16 V
2205	4822 122 31759	22 nF	
2206	4822 122 31839	82 pF	
2207	4822 124 22027	47 µF	25 V
2208	4822 124 22027	47 µF	25 V
2301	4822 122 33011	470 nF	16 V
2302	4822 122 33011	470 nF	16 V
2304	4822 122 33011	470 nF	16 V
2305	4822 122 33011	470 nF	16 V
2307	4822 122 32975	33 pF	
2308	4822 122 31759	22 nF	
2309	4822 122 31767	150 pF	
2310	4822 122 31767	150 pF	
2311	4822 122 31759	22 nF	
2312	4822 122 31839	82 pF	
2313	4822 124 22027	47 µF	25 V
2314	5322 122 31848	33 nF	
2315	4822 125 50062	10 pF	trimmer
2316	4822 122 32482	22 pF	
2318	4822 124 22027	47 µF	25 V

2319	5322 122 31848	33 nF	
2323	5322 122 31848	33 nF	
2324	4822 122 32442	10 nF	
2325	4822 122 31759	22 nF	
2501	4822 124 22028	1 µF	63 V
2502	4822 124 22028	1 µF	63 V
2503	4822 124 22028	1 µF	63 V
2504	4822 124 22028	1 µF	63 V
2505	4822 122 31969	3.3 nF	
2506	4822 122 31969	3.3 nF	
2507	4822 122 32975	33 pF	
2508	4822 122 32975	33 pF	
2509	4822 124 22188	3.3 µF	63 V
2510	4822 124 22188	3.3 µF	63 V
2511	4822 122 33009	270 nF	25 V
2512	5322 122 32839	100 nF	

2513	5322 122 32839	100 nF	
2514	4822 124 22027	47 µF	25 V
2515	4822 124 22027	47 µF	25 V
2516	4822 124 22027	47 µF	25 V
2601	4822 122 33011	470 nF	16 V
2602	4822 122 32891	68 nF	
2603	4822 122 31966	27 pF	
2604	4822 122 31759	22 nF	
2605	4822 124 22187	15 µF	63 V
2606	4822 122 32442	10 nF	
2607	4822 122 32504	15 pF	
2608	5322 122 31647	1 nF	
2609	4822 122 32975	33 pF	
2610	4822 122 31759	22 nF	
2611	4822 122 32142	270 pF	
2612	4822 122 32974	100 pF	

2613	4822 122 31773	560 pF
2614	4822 122 32976	470 pF
2615	4822 122 32442	10 nF
2616	5322 122 31848	33 nF
2617	5322 122 31848	33 nF
2618	5322 122 31848	33 nF
2619	5322 122 31848	33 nF
2620	5322 122 31848	33 nF
2621	5322 122 31848	33 nF
2622	5322 122 31848	33 nF
2623	5322 122 31848	33 nF
2624	5322 122 31848	33 nF
2625	5322 122 31848	33 nF
2627	4822 122 32504	15 pF

LIST OF ELECTRICAL PARTS MODULE W

Eproms (programmed)

7201 IC1	4822 209 51258	TMS 27128 sync
7224 IC24	4822 209 51259	TMS 27128 descrambler
7247 IC47	4822 209 51261	TMS 27128 LV DOS 1
7248 IC48	4822 209 51262	TMS 27128 LV DOS 2

Crystals

5001 X1	4822 242 71628	8MHz

Resistor networks

3003 R3	4822 116 90247	9x 220 Ω
3004 R4	4822 116 90248	9x 330 Ω
3005 R5	4822 116 90247	9x 220 Ω
3006 R6	4822 116 90248	9x 330 Ω
3007 R7	4822 116 90251	9x 3.3kΩ

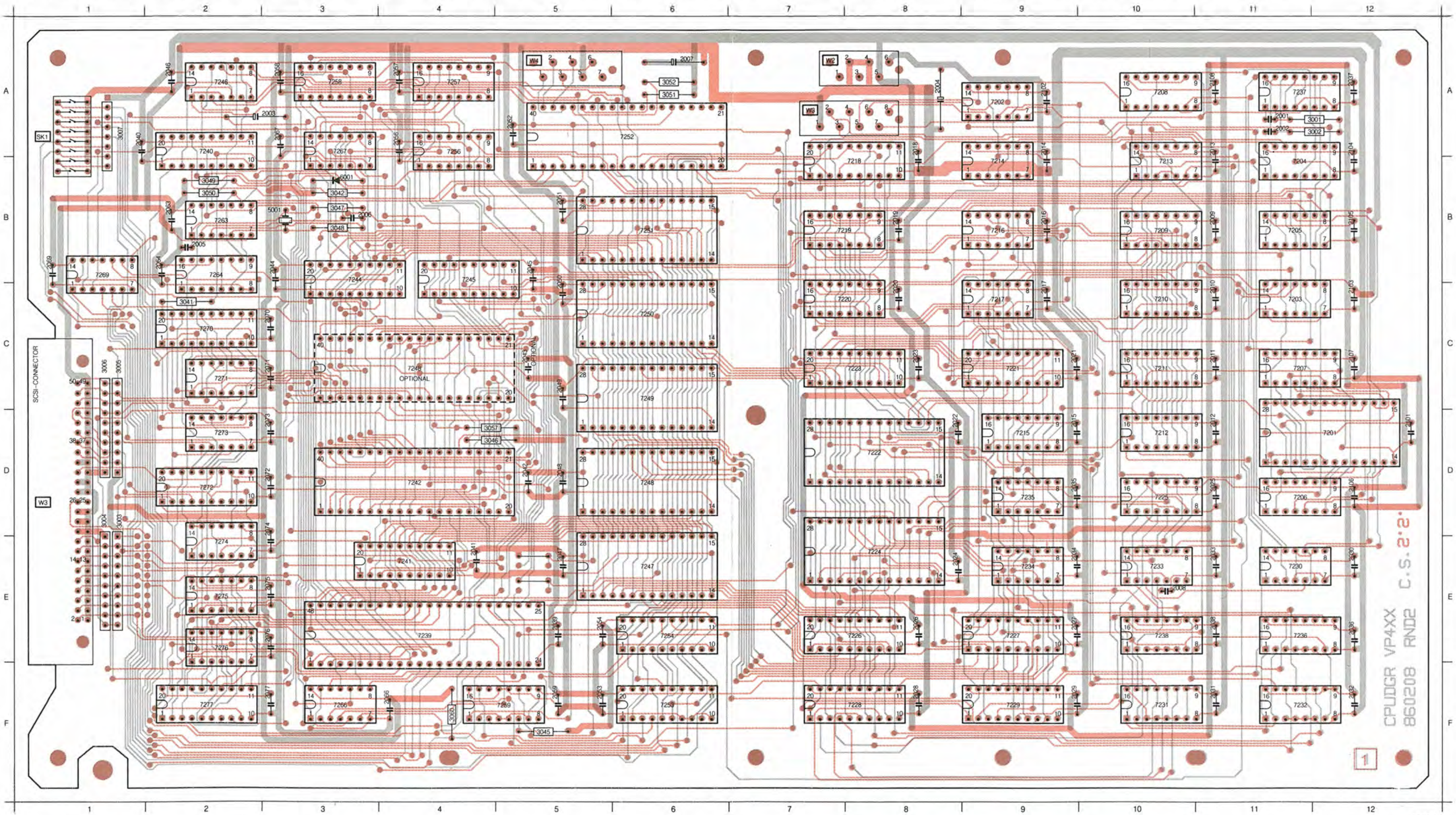
2001	c1	4822 122 31413	150 pF	
2002	c2	5322 122 32072	33 pF	
2003	c3	5322 124 21749	10 µF	63 V
2004	c4	4822 124 22027	47 µF	25 V
2005	c5	5322 122 32072	33 pF	
2006	c6	4822 122 30103	22 nF	63 V
2007	c7	4822 124 22027	47 µF	25 V
2102	c39..	4822 122 30103	22 nF	63 V
2177	..c77			

CPU+DATA GRABBER MODULE

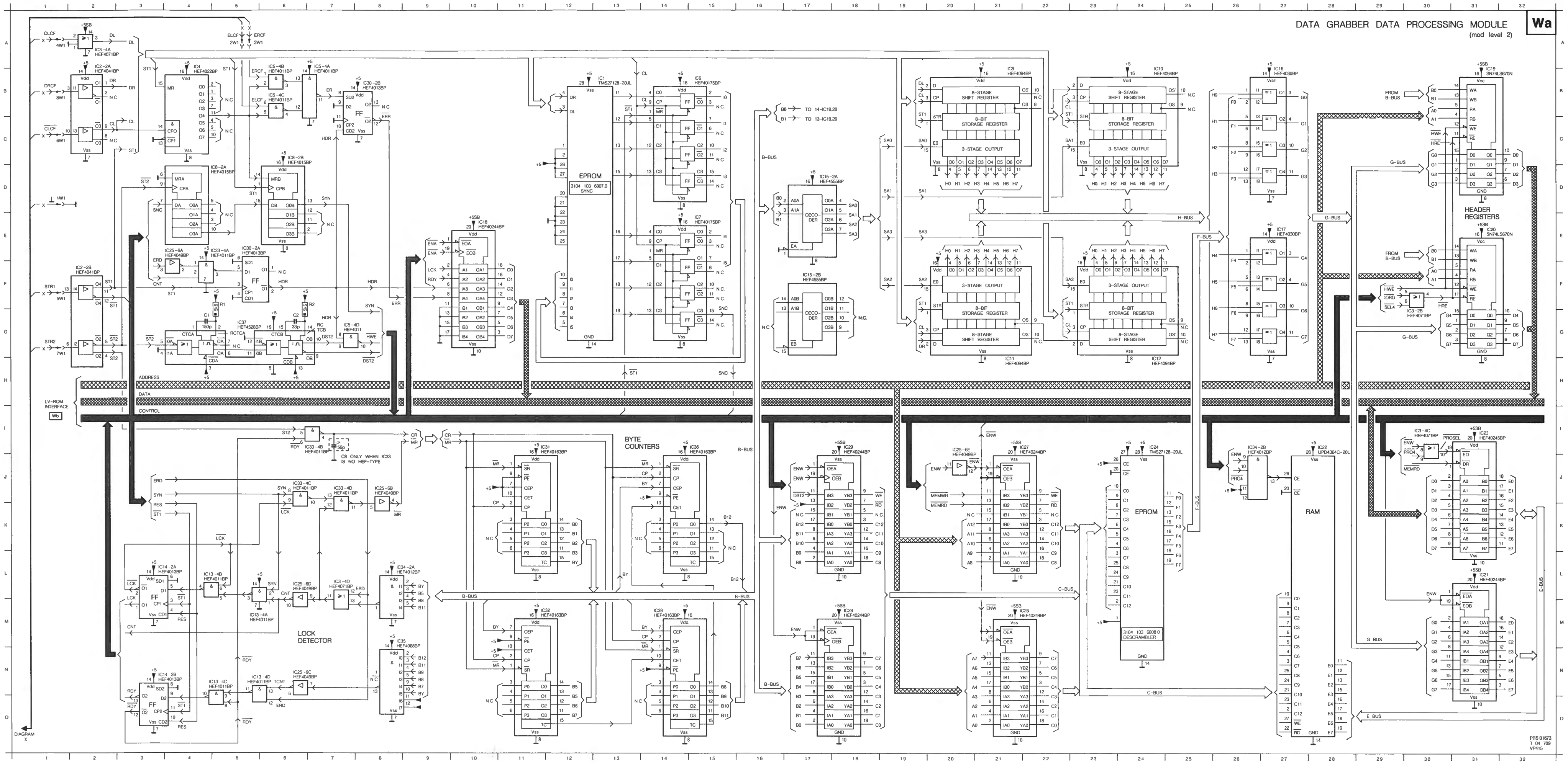
W

(MOD LEVEL 2)

2001 A11	2004 A 8	2007 A 6	2011 C11	2017 C 9	2023 C 8	2029 F 9	2035 D 9	2041 E 4	2047 E 5	2053 F 5	2063 B 2	2071 C 3	2077 F 3	3006 C 1	3047 B 3	3057 D 4	7203 C11	7209 B10	7215 D 9	7221 C 9	7227 E 9	7233 E10	7239 E 4	7246 A 2	7251 B 6	7258 A 3	7269 B 1	7275 E 2
2101 D12	2104 A12	2107 C12	2012 D11	2018 A 8	2024 E 8	2030 E12	2036 E12	2042 D 5	2048 D 5	2054 E 5	2064 B 2	2072 D 3	3001 A12	3007 A 1	3048 B 3	3060 F 4	7204 B11	7210 C10	7216 B 9	7222 D 8	7228 F 8	7234 E 9	7240 A 2	7247 E 6	7252 A 6	7259 F 5	7270 C 2	7276 E 2
2002 A11	2005 B 2	2008 E10	2013 A11	2019 B 8	2025 D11	2031 F11	2037 A12	2043 C 5	2049 C 5	2056 A 4	2066 F 4	2073 D 3	3002 A12	3041 C 2	3049 B 2	5001 B 3	7205 B11	7211 C10	7217 C 9	7223 C 8	7229 F 9	7235 D 9	7241 E 4	7248 D 6	7253 F 6	7263 B 2	7271 C 2	7277 F 2
2102 A 9	2105 B12	2108 A11	2014 A 9	2020 C 8	2026 E 8	2032 F12	2038 E11	2044 B 3	2050 B 5	2057 A 4	2067 A 3	2074 D 3	3003 D 1	3042 B 3	3050 B 2	6001 B 3	7206 D11	7212 D10	7218 B 8	7224 E 8	7230 E11	7236 E11	7242 D 4	7248 C 4	7254 E 6	7264 B 2	7272 D 2	
2003 A 3	2006 B 3	2009 B11	2015 D 9	2021 C 9	2027 E 9	2033 E11	2039 E 5	2045 B 5	2051 B 5	2058 A 3	2069 B 1	2075 E 3	3004 D 1	3045 F 5	3051 A 6	7201 D12	7207 C11	7213 B10	7219 B 8	7225 D10	7231 F10	7237 A11	7244 B 3	7249 C 6	7256 A 4	7266 F 3	7273 D 2	
2103 C12	2106 D12	2010 C11	2016 B 9	2022 D 8	2028 F 8	2034 E 9	2040 A 1	2046 A 2	2052 A 5	2059 F 5	2070 C 3	2076 E 3	3005 C 1	3046 D 4	3052 A 6	7202 A 9	7208 A10	7214 B 9	7220 C 8	7226 E 8	7232 F11	7238 E10	7245 B 4	7250 C 6	7257 A 4	7267 A 3	7274 E 2	

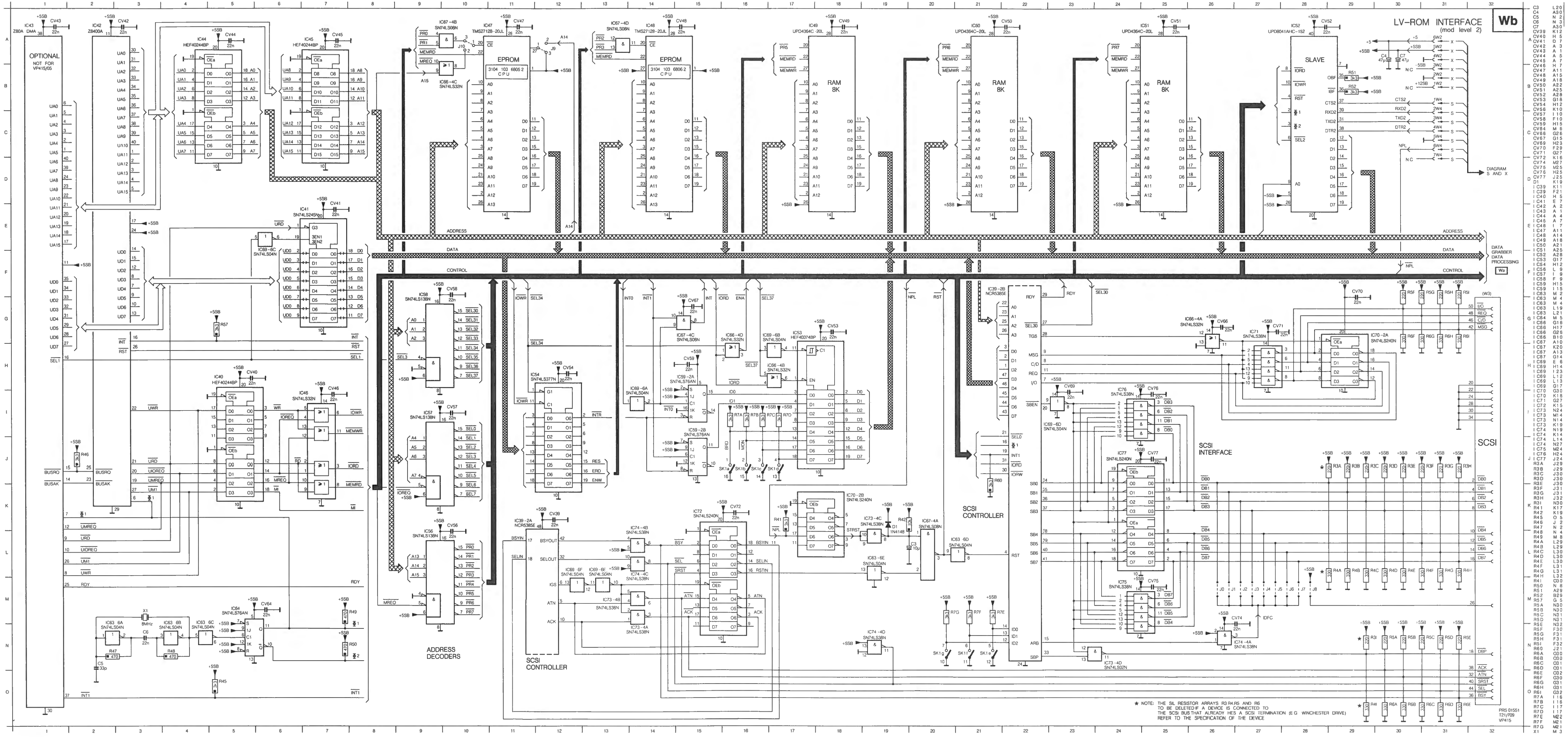


PCB 01016
T10 711



C1	G 4
C2	G 6
C8	I 7
IC1	D12
IC10	B24
IC11	H21
IC12	H24
IC13	L 4
IC13	N 5
IC13	N 5
IC13	L 5
IC14	L 4
IC14	N 4
IC15	D17
IC15	F17
IC16	B27
IC17	E27
IC18	E10
IC19	B31
IC2	F 2
IC2	A 2
IC20	E31
IC21	L31
IC22	K28
IC23	I 31
IC24	K24
IC25	E 4
IC25	I 20
IC25	L 6
IC25	N 6
IC25	J 8
IC26	M22
IC27	I 22
IC28	M18
IC29	I 18
IC3	A 2
IC3	G30
IC3	I 30
IC3	L 7
IC30	E 5
IC30	B 8
IC31	I 12
IC32	M12
IC33	E 4
IC33	J 6
IC33	J 7
IC33	I 7
IC34	I 26
IC34	L 9
IC35	M 9
IC36	I 15
IC37	G 5
IC38	M15
IC4	A 4
IC5	A 6
IC5	B 6
IC5	A 7
IC5	G 7
IC6	B15
IC7	E15
IC8	D 5
IC8	C 6
IC9	B21
R1	F 5
R2	F 7

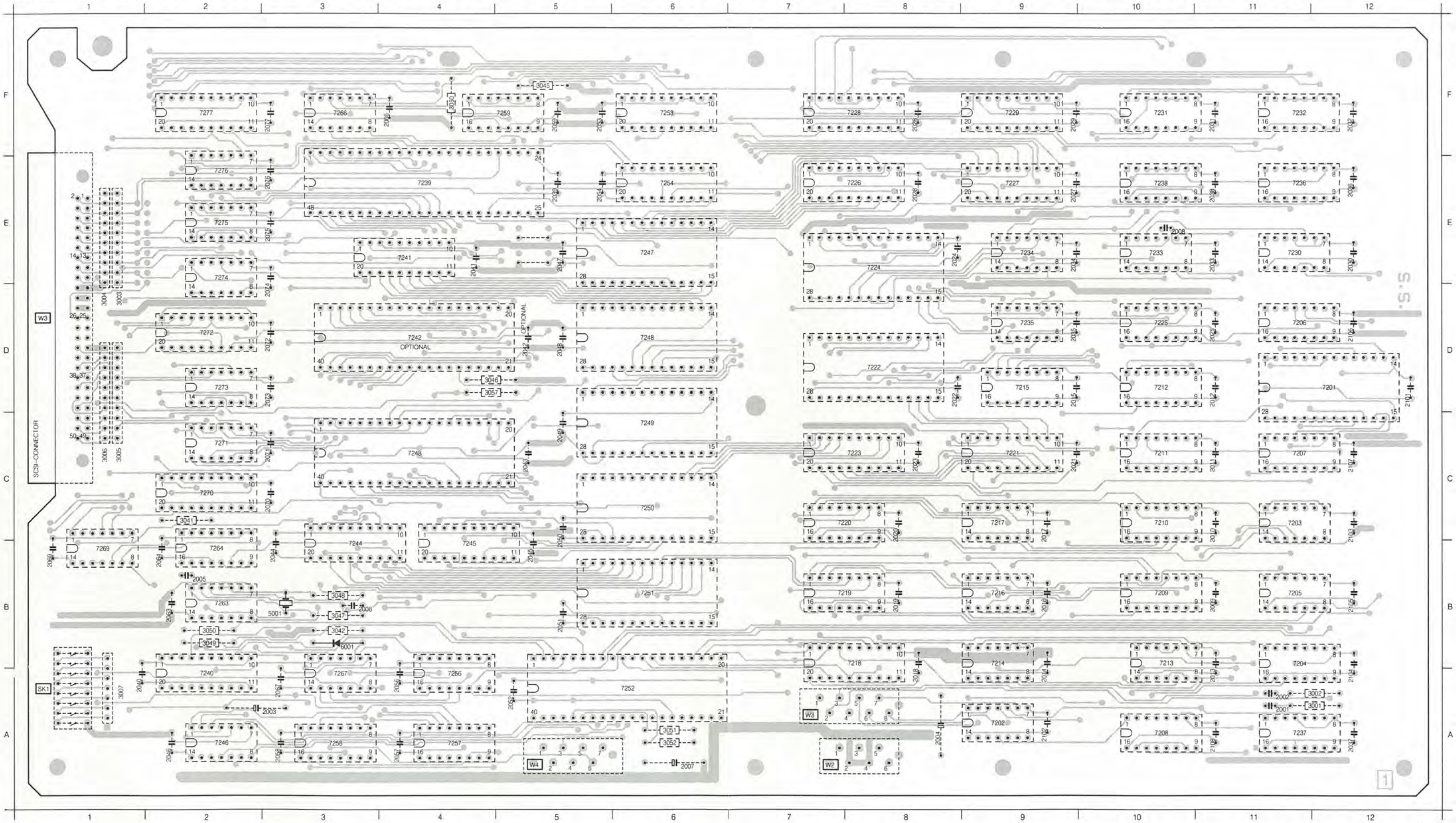
CS 6 889



LV-ROM INTERFACE
(mod level 2)
Wb
OPTIONAL
NOT FOR VP415/05
EPROM
RAM 8K
SLAVE
ADDRESS
DATA
CONTROL
DATA GRABBER DATA PROCESSING
ADDRESS DECODERS
SCSI CONTROLLER
SCSI INTERFACE
SCSI
DIAGRAM S AND X
★ NOTE: THE SIL RESISTOR ARRAYS R3,R4,R5 AND R6 TO BE DELETED IF A DEVICE IS CONNECTED TO THE SCSI BUS THAT ALREADY HAS A SCSI TERMINATION (E.G. WINCHESTER DRIVE) REFER TO THE SPECIFICATION OF THE DEVICE

CS 6 890

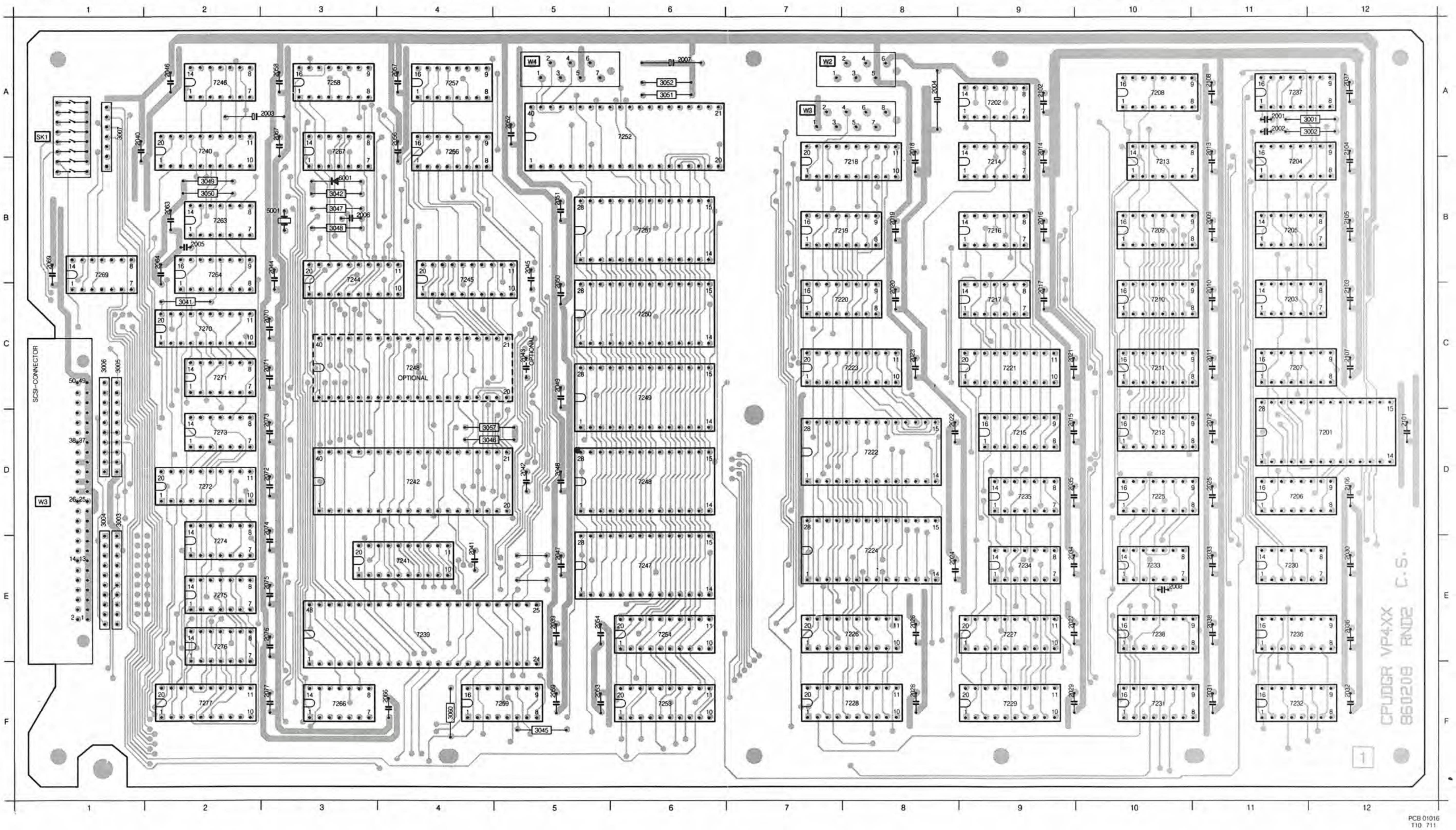
2001 A11	2004 A 8	2007 A 6	2011 C11	2017 B 9	2023 C 8	2029 F 9	2035 D 9	2041 D 4	2047 E 5	2053 F 5	2063 B 2	2071 C 3	2077 F 3	3006 C 1	3047 B 3	3057 D 4	7203 C11	7209 B10	7215 D 9	7221 C 9	7227 E 9	7233 E10	[illegible]	7247 E 6	7252 A 6	7259 F 5	7270 C 2	7276 E 2
2101 C12	2104 A12	2107 C12	2012 C11	2018 A 8	2024 E 8	2030 E12	2036 E12	2042 D 5	2048 D 5	2054 E 5	2064 B 2	2072 D 3	3001 A12	3007 A 1	3048 B 3	3060 F 4	7204 A11	7210 C10	7216 B 9	7222 D 8	7228 F 8	7234 E 9	7241 [illegible] 4	7248 D 6	7253 F 6	7263 B 2	7271 C 2	7277 F 2
2002 A11	2005 B 2	2008 E10	2013 A11	2019 B 8	2025 D11	2031 F11	2037 A12	2043 C 5	2049 C 5	2056 A 4	2066 F 4	2073 C 3	3002 A12	3041 C 2	3049 B 2	5001 B 3	7205 B11	7211 C10	7217 C 9	7223 C 8	7229 F 9	7235 D 9	7242 D 4	7248 C 4	7254 E 6	7264 B 2	7272 D 2	7239 E 4
2102 A 9	2105 B12	2108 A11	2014 A 9	2020 B 8	2026 E 8	2032 F12	2038 E11	2044 B 3	2050 B 5	2057 A 4	2067 A 3	2074 D 3	3003 D 1	3042 B 3	3050 B 2	6001 B 3	7206 D11	7212 D10	7218 A 8	7224 E 8	7230 E11	7236 E11	7244 B 3	7249 C 6	7256 A 4	7266 F 3	7273 D 2	
2003 A 3	2006 B 3	2009 B11	2015 C 9	2021 C 9	2027 E 9	2033 E11	2039 E 5	2045 B 5	2051 B 5	2058 A 3	2069 B 1	2075 E 3	3004 D 1	3045 F 5	3051 A 6	7201 D12	7207 C11	7213 A10	7219 B 8	7225 D10	7231 F10	7237 A11	7245 B 4	7250 C 6	7257 A 4	7267 A 3	7274 E 2	
2103 B12	2106 D12	2010 B11	2016 B 9	2022 C 8	2028 F 8	2034 E 9	2040 A 1	2046 A 2	2052 A 5	2059 F 5	2070 C 3	2076 E 3	3005 C 1	3046 D 4	3052 A 6	7202 A 9	7208 A10	7214 A 9	7220 C 8	7226 E 8	7232 F11	7238 E10	7246 A 2	7251 B 6	7258 A 3	7269 B 1	7275 E 2	



PCB 01016
T10 711

2001 A11	2004 A 8	2007 A 6	2011 C11	2017 C 9	2023 C 8	2029 F 9	2035 D 9	2041 E 4	2047 E 5	2053 F 5	2063 B 2	2071 C 3	2077 F 3	3006 C 1
2101 D12	2104 A12	2107 C12	2012 D11	2018 A 8	2024 E 8	2030 E12	2036 E12	2042 D 5	2048 D 5	2054 E 5	2064 B 2	2072 D 3	3001 A12	3007 A 1
2002 A11	2005 B 2	2008 E10	2013 A11	2019 B 8	2025 D11	2031 F11	2037 A12	2043 C 5	2049 C 5	2056 A 4	2066 F 4	2073 D 3	3002 A12	3041 C 2
2102 A 9	2105 B12	2108 A11	2014 A 9	2020 C 8	2026 E 8	2032 F12	2038 E11	2044 B 3	2050 B 5	2057 A 4	2067 A 3	2074 D 3	3003 D 1	3042 B 3
2003 A 3	2006 B 3	2009 B11	2015 D 9	2021 C 9	2027 E 9	2033 E11	2039 E 5	2045 B 5	2051 B 5	2058 A 3	2069 B 1	2075 E 3	3004 D 1	3045 F 5
2103 C12	2106 D12	2010 C11	2016 B 9	2022 D 8	2028 F 8	2034 E 9	2040 A 1	2046 A 2	2052 A 5	2059 F 5	2070 C 3	2076 E 3	3005 C 1	3046 D 4

3047 B 3	3057 D 4	7203 C11	7209 B10	7215 D 9	7221 C 9	7227 E 9	7233 E10	7239 E 4	7246 A 2	7251 B 6	7258 A 3	7269 B 1	7275 E 2
3048 B 3	3060 F 4	7204 B11	7210 C10	7216 B 9	7222 D 8	7228 F 8	7234 E 9	7240 A 2	7247 E 6	7252 A 6	7259 F 5	7270 C 2	7276 E 2
3049 B 2	5001 B 3	7205 B11	7211 C10	7217 C 9	7223 C 8	7229 F 9	7235 D 9	7241 E 4	7248 D 6	7253 F 6	7263 B 2	7271 C 2	7277 F 2
3050 B 2	6001 B 3	7206 D11	7212 D10	7218 B 8	7224 E 8	7230 E11	7236 E11	7242 D 4	7248 C 4	7254 E 6	7264 B 2	7272 D 2	
3051 A 6	7201 D12	7207 C11	7213 B10	7219 B 8	7225 D10	7231 F10	7237 A11	7244 B 3	7249 C 6	7256 A 4	7266 F 3	7273 D 2	
3052 A 6	7202 A 9	7208 A10	7214 B 9	7220 C 8	7226 E 8	7232 F11	7238 E10	7245 B 4	7250 C 6	7257 A 4	7267 A 3	7274 E 2	



LV ROM DEC MODULE X

(MOD. LEVEL 3)

2501 B 5	2515 B 5	2541 C 6	2604 A 2	2710 B 2	2715 C 1	5503 C 5	5507 C 6	5702 A 1	6510 C 4	6545 A 5	6562 B 6	6601 A 3	6605 B 2
2502 B 4	2519 B 4	2543 C 5	2605 B 2	2711 C 2	2716 C 1	5504 D 3	5508 D 5	5703 B 1	6512 B 4	6549 A 5	6563 B 6	6602 B 3	6606 B 3
2507 C 5	2527 A 5	2602 B 3	2705 B 1	2712 C 1	2717 C 2	5505 B 3	5601 C 3	5704 B 1	6540 B 5	6550 A 5	6564 C 6	6603 D 2	6704 C 1
2513 D 3	2540 C 6	2603 A 3	2708 B 2	2714 C 2	5501 B 4	5506 C 6	5701 A 1	6501 B 5	6544 A 5	6551 A 5	6565 B 6	6604 C 2	6705 C 1

2503 B 5	2520 A 5	2545 B 6	2701 A 2	3502 B 5	3510 B 4	3523 A 6	3533 D 4	3541 A 4	3552 C 6	3607 B 3	3616 C 3	3706 B 1	3714 C 1	3722 D 1	6702 C 1
2505 B 5	2521 A 5	2546 B 6	2702 A 2	3503 B 5	3511 B 4	3525 A 6	3534 A 5	3542 A 5	3555 D 4	3608 B 2	3617 C 2	3707 B 1	3715 C 2	3723 C 1	6703 C 1
2506 B 4	2522 B 6	2601 A 2	2703 B 2	3504 B 5	3512 B 5	3527 A 6	3535 A 5	3543 A 5	3601 A 3	3609 A 2	3618 D 2	3708 B 1	3716 C 1	3831 D 4	6706 D 1
2508 B 5	2523 A 5	2606 B 2	2704 B 2	3505 B 5	3514 D 4	3528 B 6	3536 A 5	3544 A 4	3602 B 3	3610 A 2	3701 A 1	3709 B 1	3717 C 1	3835 B 5	
2509 B 5	2525 A 5	2607 B 3	2706 B 2	3506 B 6	3515 B 6	3529 A 6	3537 A 5	3545 A 4	3603 A 3	3612 A 2	3702 A 1	3710 B 1	3718 D 1	3938 B 4	
2511 C 5	2538 B 3	2608 B 3	2707 B 1	3507 B 4	3516 B 5	3530 A 5	3538 A 4	3549 B 4	3604 B 3	3613 B 2	3703 B 2	3711 B 1	3719 D 1	6530 A 6	
2512 A 5	2539 D 3	2609 C 2	2709 B 1	3508 B 4	3520 A 6	3531 B 5	3539 A 4	3550 C 6	3605 B 2	3614 B 2	3704 B 1	3712 C 2	3720 D 1	6531 A 6	
2514 B 6	2542 C 6	2610 C 2	2713 C 1	3509 B 5	3521 A 5	3532 B 6	3540 B 4	3551 C 6	3606 B 2	3615 B 3	3705 B 1	3713 C 1	3721 C 2	6701 B 1	

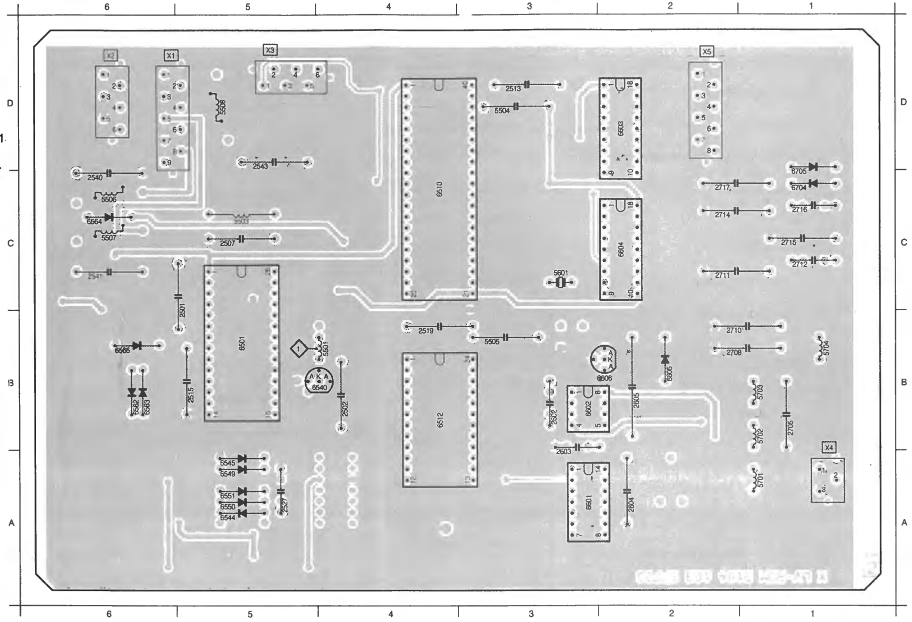
ADJUSTMENTS

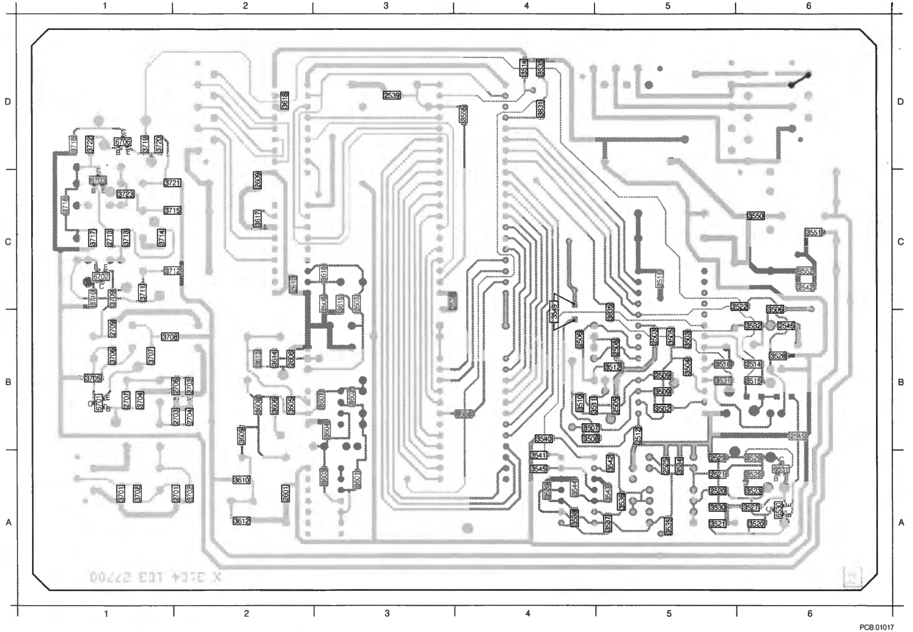
Required
Frequency counter

Adjustment conditions
Stand–by position of the set

Adjustments

1) L5501 (Demod. freq.)
   - Short–circuit pin 6–IC6501 to ground.
   - Measure with the frequency counter on 22–IC6501 (clock)
   - Adjust L5501 for a frequency of 4.32 MHz ± 1 kHz. (the voltage on junction R3510/R3511 should than be 5 V ± 0.1 V).
   - Remove the short circuit of pin 6.





PCB 01017
T03/718

LIST OF ELECTRICAL PARTS MODULE X

Crystals

5601	4822 242 71461	4.2336 MHz

Coils

5501	4822 156 21155	7.95 µH
5503	4822 156 20966	47 µH
5504	4822 156 20966	47 µH
5505	4822 156 20966	47 µH
5506	4822 158 10101	5.3 µH
5507	4822 158 10101	5.3 µH
5508	4822 158 10101	5.3 µH
5701	4822 156 21026	34 µH
5702	4822 156 11005	42.5 µH
5703	4822 156 11005	42.5 µH
5704	4822 156 21113	52 µH

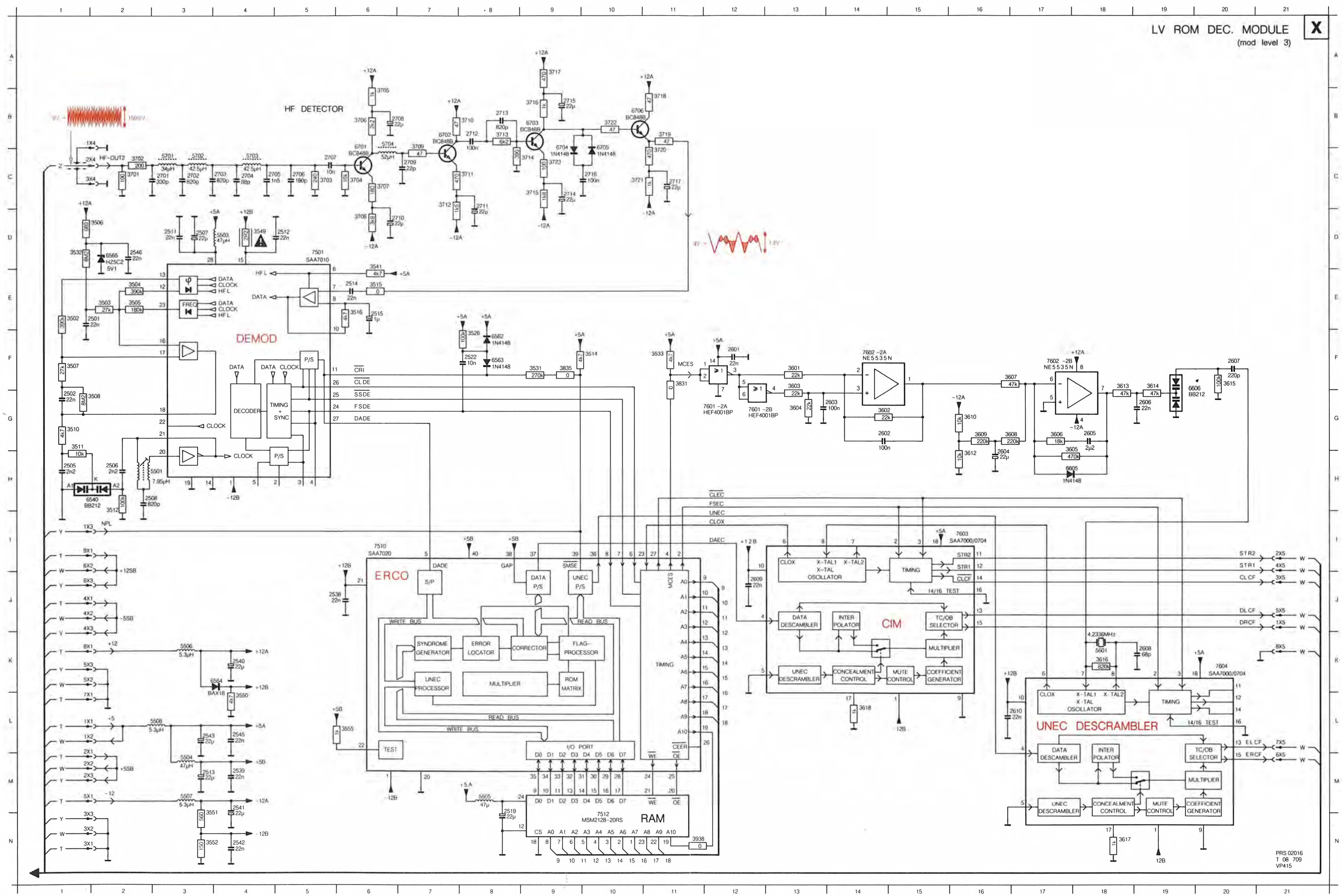
NFR25 Resistors

3549	4822 111 30492	2.2 Ω

2501	4822 121 51099	22 nF	63 V
2502	4822 121 51099	22 nF	63 V
2505	4822 122 31644	2.2 nF	
2506	4822 122 31644	2.2 nF	
2507	5322 124 21643	22 µF	40 V
2508	4822 122 31974	820 pF	
2511	4822 122 31759	22 nF	
2512	4822 122 31759	22 nF	
2513	5322 124 21643	22 µF	40 V
2514	4822 122 31759	22 nF	
2515	4822 124 22028	1 µF	63 V
2519	5322 124 21643	22 µF	40 V
2520	4822 122 32976	470 pF	
2521	4822 122 32976	470 pF	
2522	4822 122 32442	10 nF	
2523	4822 122 31759	22 nF	
2525	4822 122 31644	2.2 nF	
2527	4822 121 41608	100 nF	100 V
2538	4822 122 31759	22 nF	
2539	4822 122 31759	22 nF	
2540	5322 124 21643	22 µF	40 V
2541	5322 124 21643	22 µF	40 V
2542	4822 122 31759	22 nF	
2543	5322 124 21643	22 µF	40 V
2545	4822 122 31759	22 nF	
2546	4822 122 31759	22 nF	
2601	4822 122 31759	22 nF	
2602	4822 121 41608	100 nF	100 V
2603	4822 121 41608	100 nF	100 V
2604	5322 124 21643	22 µF	40 V
2605	4822 121 41936	2.2 µF	10% 100 V
2606	4822 122 31759	22 nF	
2607	4822 122 31965	220 pF	
2608	4822 122 33002	68 pF	
2609	4822 122 31759	22 nF	
2610	4822 122 31759	22 nF	
2701	4822 121 42915	330 pF	
2702	4822 122 31974	820 pF	
2703	4822 122 31974	820 pF	
2704	4822 122 33002	68 pF	
2705	4822 121 50632	1.5 nF	250 V
2706	4822 122 31768	180 pF	
2707	4822 122 32442	10 nF	
2708	5322 124 21643	22 µF	40 V
2709	4822 122 32482	22 pF	
2710	5322 124 21643	22 µF	40 V
2711	5322 124 21643	22 µF	40 V
2712	4822 121 41608	100 nF	100 V
2713	4822 122 31974	820 pF	
2714	5322 124 21643	22 µF	40 V
2715	5322 124 21643	22 µF	40 V
2716	4822 121 41608	100 nF	100 V
2717	5322 124 21643	22 µF	40 V

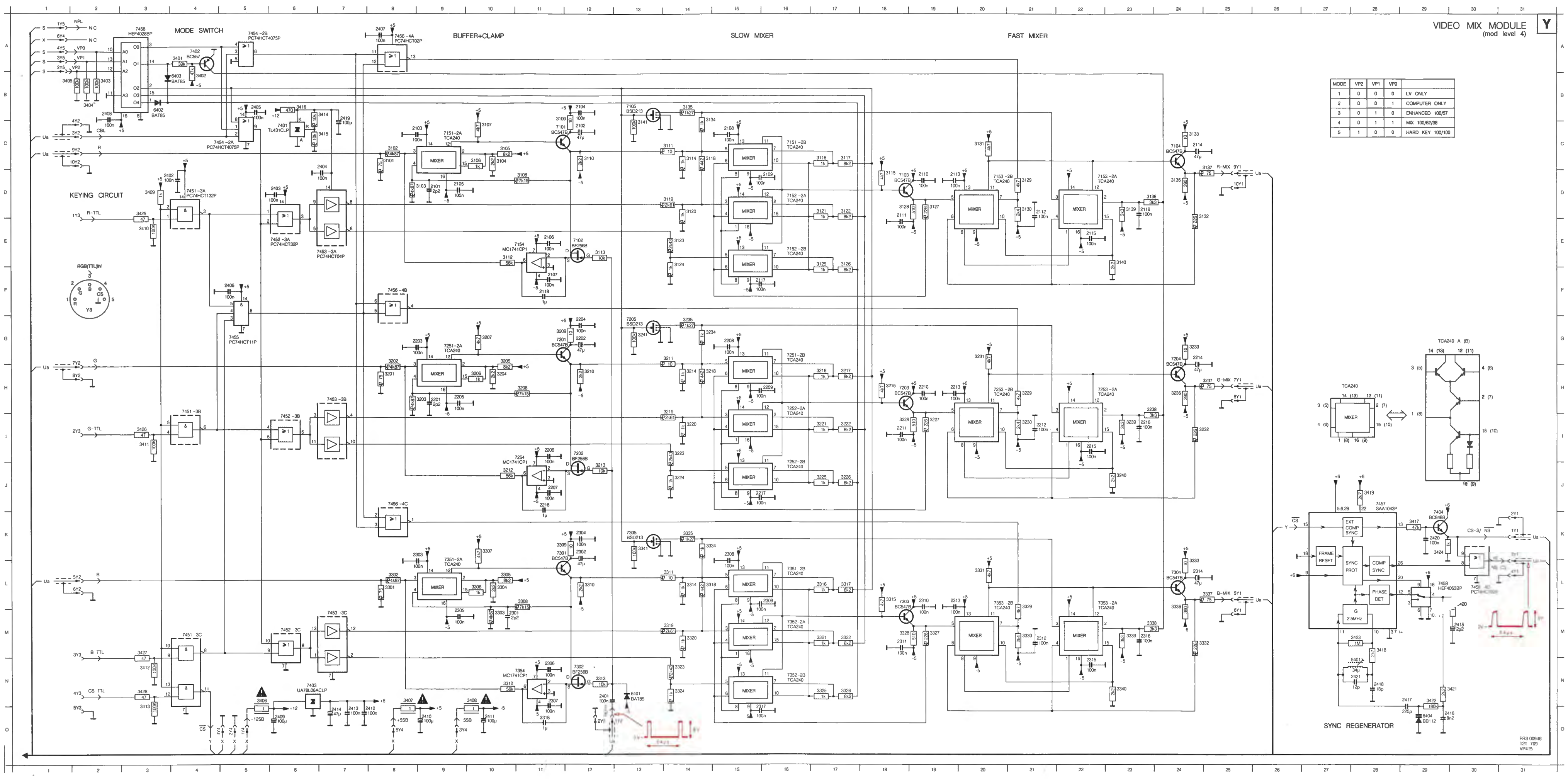
2501	E 2	2511	D 3	2522	F 8	2543	L 3	2604	H16	2610	L17	2706	C 5	2712	B 8	3502	E 1	3508	G 2	3516	E 6	3549	D 4	3602	G14
2502	G 1	2512	D 5	2538	J 6	2545	L 4	2605	G18	2701	C 3	2707	C 5	2713	B 8	3503	E 2	3510	G 1	3526	F 8	3550	L 4	3603	F13
2505	H 1	2513	M 3	2539	M 4	2546	D 2	2606	G19	2702	C 3	2708	B 7	2714	C 9	3504	E 2	3511	G 1	3531	F 9	3551	M 4	3604	G13
2506	H 2	2514	E 6	2540	K 4	2601	F12	2607	F20	2703	C 4	2709	C 7	2715	B 9	3505	E 2	3512	H 2	3532	D 1	3552	N 4	3605	G17
2507	D 3	2515	E 6	2541	M 4	2602	G14	2608	K19	2704	C 4	2710	D 7	2716	C10	3506	D 2	3514	F10	3533	F11	3555	L 6	3606	G17
2508	H 3	2519	M 8	2542	N 4	2603	G14	2609	J12	2705	C 5	2711	C 8	2717	C11	3507	F 1	3515	E 6	3541	D 6	3601	F13	3607	F17

3608	G17	3615	F20	3703	C 5	3709	B 7	3715	C 9	3721	C10	5501	H 3	5508	L 3	6540	H 2	6606	F20	6706	B10	7602	F17
3609	G16	3616	K18	3704	C 6	3710	B 8	3716	B 9	3722	B10	5503	D 4	5601	K18	6562	F 8	6701	B 6	7501	D 5	7602	F14
3610	G16	3617	N18	3705	B 6	3711	C 8	3717	A 9	3723	C 9	5504	M 3	5701	C 3	6563	F 8	6702	B 7	7510	I 6	7603	I 16
3612	H16	3618	L14	3706	B 6	3712	C 7	3718	B11	3831	F11	5505	M 8	5702	C 3	6564	K 4	6703	B 9	7512	N10	7604	K20
3613	F18	3701	C 2	3707	C 6	3713	B 8	3719	B11	3835	F 9	5506	K 3	5703	C 4	6565	D 2	6704	B 9	7601	G12		
3614	F19	3702	C 2	3708	D 6	3714	C 9	3720	C11	3938	N11	5507	M 3	5704	B 6	6605	H17	6705	B10	7601	G12		



CS 6 891

VIDEO MIX MODULE (mod level 4)



2101	D 9	3230	I 21
2102	C12	3231	G20
2103	C 9	3232	I 25
2104	B12	3233	G24
2105	D 9	3234	G15
2106	E11	3235	G14
2107	F11	3236	H24
2108	C15	3237	H25
2109	D16	3238	H23
2110	D19	3239	I 23
2111	D18	3240	J23
2112	D21	3241	G13
2113	D19	3301	L 8
2114	C24	3302	L 8
2115	E22	3303	M10
2116	D23	3304	L10
2117	F15	3305	L10
2118	F11	3306	L10
2201	H 9	3307	K10
2202	G12	3308	L11
2203	G 9	3309	K11
2204	G12	3310	L12
2205	H 9	3311	L14
2206	I 11	3312	N10
2207	J11	3313	N12
2208	G15	3314	L14
2209	H16	3315	L18
2210	H19	3316	L17
2211	I 18	3317	L17
2212	I 21	3318	L15
2213	H19	3319	M14
2214	G24	3320	M14
2215	I 22	3321	M17
2216	I 23	3322	M17
2217	J15	3323	N14
2218	J11	3324	N14
2301	M11	3325	N17
2302	K12	3326	N17
2303	K 9	3327	M19
2304	K12	3328	M18
2305	M 9	3329	L21
2306	N11	3330	M21
2307	N11	3331	L20
2308	K15	3332	M25
2309	L16	3333	L24
2310	L19	3334	K15
2311	M18	3335	K14
2312	M21	3336	L24
2313	L19	3337	L25
2314	L24	3338	M23
2315	N22	3339	M23
2316	M23	3340	N23
2317	O15	3341	K13
2318	O11	3401	A 4
2401	N12	3402	B 4
2402	D 4	3403	B 2
2403	D 6	3404	B 2
2404	C 7	3405	B 1
2405	B 5	3406	N 5
2406	F 5	3407	N 8
2407	A 8	3408	N10
2408	B 2	3409	D 3
2409	O 6	3410	E 3
2410	O 9	3411	I 3
2411	O10	3412	N 3
2412	O 8	3413	N 3
2413	O 7	3414	B 7
2414	O 7	3415	C 7
2415	M30	3416	B 6
2416	O30	3417	K29
2417	N29	3418	M28
2418	N28	3419	J28
2419	B 7	3420	L30
2420	K29	3421	N30
2421	N28	3422	N29
3101	C 8	3423	M28
3102	C 8	3424	K29
3103	D 9	3425	D 3
3104	C10	3426	I 3
3105	C10	3427	M 3
3106	C10	3428	N 3
3107	C10	5401	N28
3108	D11	6401	N13
3109	B11	6402	B 3
3110	C12	6403	B 4
3111	C14	6404	O29
3112	E10	7101	C11
3113	E12	7102	E12
3114	C14	7103	D18
3115	D18	7104	C24
3116	C17	7105	B13
3117	C17	7151	C 9
3118	C15	7151	C16
3119	D14	7152	D16
3120	D14	7152	E16
3121	D17	7153	D20
3122	D17	7153	D22
3123	E14	7154	E11
3124	E14	7201	G11
3125	E17	7202	I 12
3126	E17	7203	H18
3127	D19	7204	G24
3128	D18	7205	G13
3129	D21	7251	G 9
3130	D21	7251	G16
3131	C20	7252	H16
3132	D25	7252	J16
3133	C24	7253	H20
3134	B15	7253	H22
3135	B14	7254	I 11
3136	D24	7301	K11
3137	C25	7302	N12
3138	D23	7303	L18
3139	D23	7304	L24
3140	E23	7305	K13
3141	C13	7351	K 9
3201	H 8	7351	L16
3202	G 8	7352	M16
3203	H 9	7352	N16
3204	H10	7353	L20
3205	G10	7353	L22
3206	H10	7354	N11
3207	G10	7401	C 6
3208	H11	7402	A 4
3209	G11	7403	N 6
3210	H12	7404	K29
3211	G14	7451	D 4
3212	J10	7451	H 4
3213	J12	7451	M 4
3214	H14	7452	E 6
3215	H18	7452	I 6
3216	H17	7452	M 6
3217	H17	7453	E 7
3218	H15	7453	H 7
3219	H14	7453	M 7
3220	I 14	7454	C 5
3221	I 17	7454	A 5
3222	I 17	7455	G 5
3223	I 14	7456	A 8
3224	J14	7456	L30
3225	J17	7456	F 8
3226	J17	7456	J 8
3227	I 19	7457	J28
3228	I 18	7458	A 3
3229	H21	7459	L29

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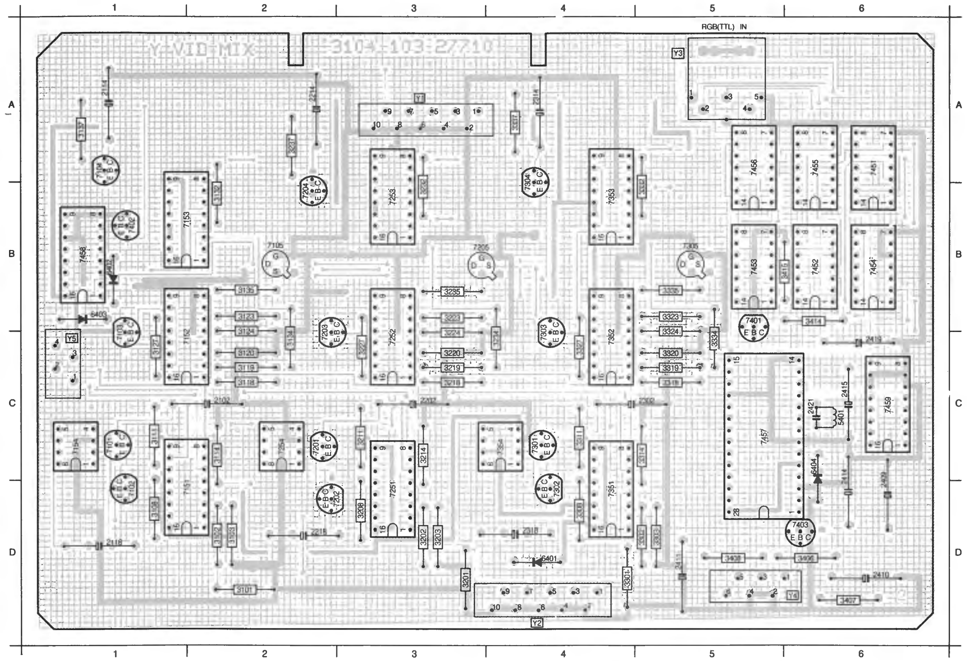
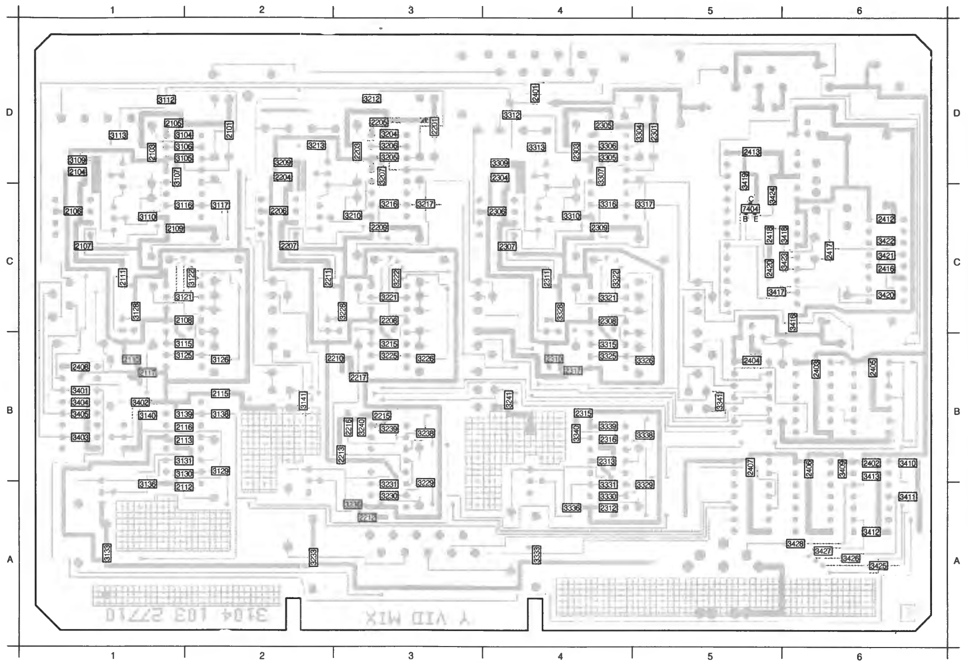
VID MIX MODULE Y

(MOD LEVEL 4)

2102 C 2	2314 A 4	2419 C 6	3114 C 2	3132 B 2	3208 D 3	3224 C 3	3302 D 5	3320 C 5	3337 A 4	6402 B 1	7105 B 2	7203 B 2	7301 C 4	7353 B 4	7453 B 5
2114 A 1	2318 D 4	2421 C 6	3118 C 2	3134 C 2	3211 C 3	3227 C 3	3303 D 5	3323 B 5	3406 D 6	6403 B 1	7151 D 1	7204 B 2	7302 D 4	7354 C 4	7454 B 6
2118 D 1	2409 C 6	3101 D 2	3119 C 2	3135 B 2	3214 C 3	3232 B 3	3308 D 4	3324 B 5	3407 D 6	6404 C 6	7152 C 1	7205 B 3	7303 B 4	7401 B 5	7455 A 6
2202 C 3	2410 D 6	3102 D 2	3120 C 2	3137 A 1	3218 C 3	3234 C 4	3311 C 4	3327 C 4	3408 D 5	7101 C 1	7153 B 1	7251 D 3	7304 A 4	7402 B 1	7456 A 5
2214 A 2	2411 D 5	3103 D 2	3123 B 2	3201 D 3	3219 C 3	3235 B 3	3314 C 5	3332 B 5	3414 B 6	7102 D 1	7154 C 1	7252 C 3	7305 B 5	7403 D 6	7457 C 5
2218 D 2	2414 C 6	3108 D 1	3124 B 2	3202 D 3	3220 C 3	3237 A 2	3318 C 5	3334 C 5	3415 B 6	7103 B 1	7201 C 2	7253 B 3	7351 D 4	7451 A 6	7458 B 1
2302 C 5	2415 C 6	3111 C 1	3127 C 1	3203 D 3	3223 B 3	3301 D 4	3319 C 5	3335 B 5	6401 D 4	7104 A 1	7202 D 2	7254 C 2	7352 C 4	7452 B 6	7459 C 6



2101 D 2	2112 A 2	2207 C 2	2301 D 5	2312 A 4	2406 A 6	3105 D 2	3121 C 2	3138 B 2	3212 D 3	3229 A 3	3305 D 4	3321 C 4	3338 B 5	3410 B 6	3422 C 6
2103 D 1	2113 B 2	2208 C 3	2303 D 4	2313 B 4	2407 A 5	3106 D 2	3122 C 2	3139 B 2	3213 D 2	3230 A 3	3306 D 4	3322 C 4	3339 B 4	3411 A 6	3423 C 6
2104 D 1	2115 B 2	2209 C 3	2304 D 4	2315 B 4	2408 B 1	3107 C 1	3125 B 2	3140 B 1	3215 B 3	3231 A 3	3307 C 4	3325 B 4	3340 B 4	3412 A 6	3424 C 5
2105 D 1	2116 B 2	2210 B 3	2305 D 4	2316 B 4	2412 C 6	3109 D 1	3126 B 2	3141 B 2	3216 C 3	3233 A 2	3309 D 4	3326 B 5	3341 B 5	3413 B 6	3425 A 6
2106 C 1	2117 B 1	2211 C 2	2306 C 4	2317 B 4	2413 D 5	3110 C 1	3128 C 1	3204 D 3	3217 C 3	3236 A 3	3310 C 4	3328 C 4	3401 B 1	3416 B 6	3426 A 6
2107 C 1	2201 D 3	2212 A 3	2307 C 4	2401 D 4	2416 C 6	3112 D 1	3129 B 2	3205 D 3	3221 C 3	3238 B 3	3312 D 4	3329 A 5	3402 B 1	3417 C 5	3427 A 6
2108 C 2	2203 D 3	2213 B 3	2308 C 4	2402 B 6	2417 C 6	3113 D 1	3130 B 2	3206 D 3	3222 C 3	3239 B 3	3313 D 4	3330 A 4	3403 B 1	3418 C 6	3428 A 6
2109 C 1	2204 D 2	2215 B 3	2309 C 4	2403 B 6	2418 C 5	3115 B 2	3131 B 2	3207 C 3	3225 B 3	3240 B 3	3315 B 4	3331 A 4	3404 B 1	3419 C 5	7404 C 5
2110 B 1	2205 D 3	2216 B 3	2310 B 4	2404 B 5	2420 C 5	3116 C 2	3133 A 1	3209 D 2	3226 B 3	3241 B 4	3316 C 4	3333 A 4	3405 B 1	3420 C 6	
2111 C 1	2206 C 2	2217 B 3	2311 C 4	2405 B 6	3104 D 2	3117 C 2	3136 A 1	3210 C 3	3228 C 3	3304 D 5	3317 C 5	3336 A 4	3409 A 6	3421 C 6	



PCB.01018
T10 718

LIST OF ELECTRICAL PARTS MODULE Y

Coils

5401	4822 156 21026	34 μH

NFR25 Resistors

3406	4822 111 30483	1 Ω
3407	4822 111 30483	1 Ω
3408	4822 111 30483	1 Ω

2101	4822 122 32425	2.2 pF	
2102	4822 124 22027	47 μF	25 V
2103	5322 122 32839	100 nF	
2104	5322 122 32839	100 nF	
2105	5322 122 32839	100 nF	
2106	5322 122 32839	100 nF	
2107	5322 122 32839	100 nF	
2108	5322 122 32839	100 nF	
2109	5322 122 32839	100 nF	
2110	5322 122 32839	100 nF	
2111	5322 122 32839	100 nF	
2112	5322 122 32839	100 nF	
2113	5322 122 32839	100 nF	
2114	4822 124 22027	47 μF	25 V
2115	5322 122 32839	100 nF	
2116	5322 122 32839	100 nF	
2117	5322 122 32839	100 nF	
2118	4822 121 41719	1 μF	10% 100 V
2201	4822 122 32425	2.2 pF	
2202	4822 124 22027	47 μF	25 V
2203	5322 122 32839	100 nF	
2204	5322 122 32839	100 nF	
2205	5322 122 32839	100 nF	
2206	5322 122 32839	100 nF	
2207	5322 122 32839	100 nF	
2208	5322 122 32839	100 nF	
2209	5322 122 32839	100 nF	
2210	5322 122 32839	100 nF	
2211	5322 122 32839	100 nF	
2212	5322 122 32839	100 nF	
2213	5322 122 32839	100 nF	
2214	4822 124 22027	47 μF	25 V
2215	5322 122 32839	100 nF	
2216	5322 122 32839	100 nF	
2217	5322 122 32839	100 nF	
2218	4822 121 41719	1 μF	10% 100 V
2301	4822 122 32425	2.2 pF	
2302	4822 124 22027	47 μF	25 V
2303	5322 122 32839	100 nF	
2304	5322 122 32839	100 nF	
2305	5322 122 32839	100 nF	
2306	5322 122 32839	100 nF	
2307	5322 122 32839	100 nF	
2308	5322 122 32839	100 nF	
2309	5322 122 32839	100 nF	
2310	5322 122 32839	100 nF	
2311	5322 122 32839	100 nF	
2312	5322 122 32839	100 nF	
2313	5322 122 32839	100 nF	
2314	4822 124 22027	47 μF	25 V
2315	5322 122 32839	100 nF	
2316	5322 122 32839	100 nF	
2317	5322 122 32839	100 nF	
2318	4822 121 41719	1 μF	10% 100 V
2401	5322 122 32839	100 nF	
2402	5322 122 32839	100 nF	
2403	5322 122 32839	100 nF	
2404	5322 122 32839	100 nF	
2405	5322 122 32839	100 nF	
2406	5322 122 32839	100 nF	
2407	5322 122 32839	100 nF	
2408	5322 122 32839	100 nF	
2409	5322 124 21711	100 μF	25 V
2410	5322 124 21711	100 μF	25 V
2411	5322 124 21711	100 μF	25 V
2412	5322 122 32839	100 nF	
2413	5322 122 32839	100 nF	
2414	4822 124 22027	47 μF	25 V
2415	4822 124 22029	2.2 μF	63 V
2416	4822 122 32856	8.2 nF	
2417	4822 122 31965	220 pF	
2418	4822 122 31769	18 pF	
2419	5322 124 21711	100 μF	25 V
2420	5322 122 32839	100 nF	
2421	4822 122 31056	12 pF	

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2001	D 5	2026	A 3	2042	C 5	2055	B 1	3009	C 5	3038	B 4	3054	C 5	3064	C 6	3074	C 6	3089	D 6	3101	D 6	3111	D 5	6001	C 4	6014	D 6	7005	D 5	7202	C 6
2002	C 5	2031	C 5	2043	C 5	2056	B 1	3010	D 5	3039	B 5	3055	B 5	3065	C 6	3075	C 5	3090	D 6	3102	D 6	3112	D 5	6002	D 4	6015	D 6	7010	B 5	7203	C 5
2003	D 5	2032	B 5	2044	C 5	3001	D 5	3011	C 5	3040	B 2	3056	B 5	3066	C 1	3076	C 2	3091	D 6	3103	D 6	3113	D 5	6003	C 4	6016	D 6	7011	B 5	7204	D 6
2004	D 2	2033	B 5	2045	C 5	3002	D 5	3012	C 5	3041	B 5	3057	B 6	3067	C 5	3077	C 5	3092	D 6	3104	D 5	3114	C 5	6005	D 4	6017	D 5	7012	A 5	7205	D 6
2005	D 2	2034	C 6	2048	D 6	3003	D 5	3013	C 5	3042	B 4	3058	B 1	3068	C 5	3078	C 5	3093	D 6	3105	D 5	3115	D 5	6007	B 6	6018	D 5	7013	C 5	7206	D 5
2006	D 5	2035	C 6	2049	D 6	3004	C 5	3014	D 5	3043	B 4	3059	C 6	3069	C 6	3079	C 1	3094	D 6	3106	D 5	3116	D 5	6008	C 5	6019	D 5	7015	D 6	7207	D 5
2007	D 5	2036	C 6	2051	C 1	3005	D 5	3015	D 5	3044	B 5	3060	C 6	3070	C 5	3085	A 4	3095	D 6	3107	D 5	3120	C 6	6009	C 5	7001	D 5	7016	C 5		
2023	B 5	2037	C 6	2052	C 6	3006	D 5	3019	D 4	3045	A 4	3061	C 6	3071	C 6	3086	D 6	3096	D 6	3108	D 5	3121	D 6	6010	C 6	7002	D 5	7017	D 6		
2024	B 2	2038	C 6	2053	D 1	3007	D 5	3023	C 5	3046	A 4	3062	C 6	3072	C 6	3087	D 6	3097	D 6	3109	C 5	3122	C 6	6011	C 4	7003	C 5	7018	D 5		
2025	B 3	2039	C 6	2054	C 6	3008	C 5	3037	B 5	3053	B 5	3063	C 6	3073	C 6	3088	D 2	3100	D 6	3110	C 6	3123	C 6	6013	D 6	7004	C 4	7201	B 6		

LIST OF ELECTRICAL PARTS MODULE Z

Diodes

	4822 130 60493	Detector diode
6020	4822 130 32114	GP1S04 Photo interruptor

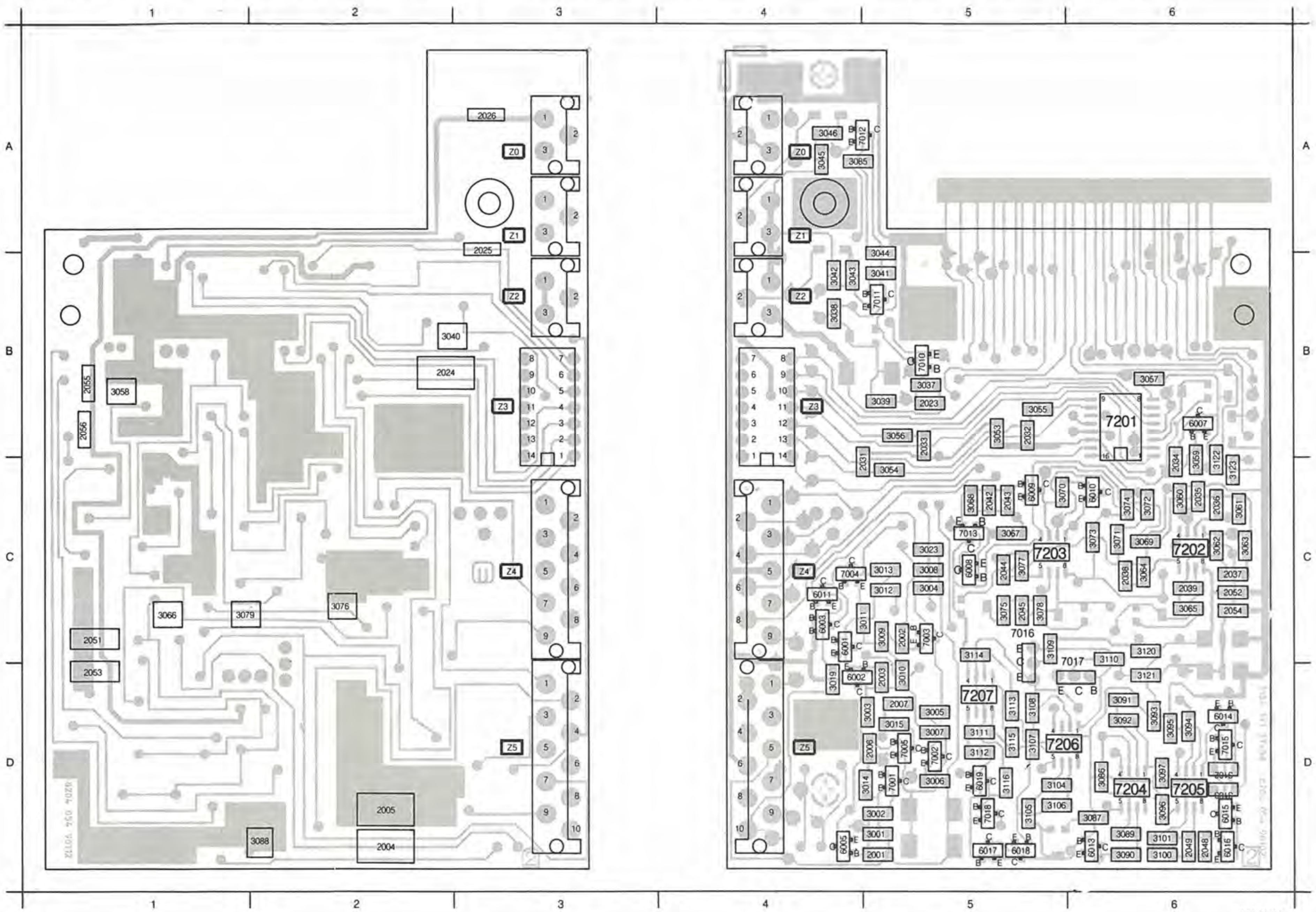
Potentiometers

3040	4822 100 11152	1 kΩ
3058	4822 100 11152	1 kΩ
3066	4822 100 11156	100 kΩ
3076	4822 100 11154	10 kΩ
3079	4822 100 11155	22 kΩ
3088	4822 100 11153	4.7 kΩ

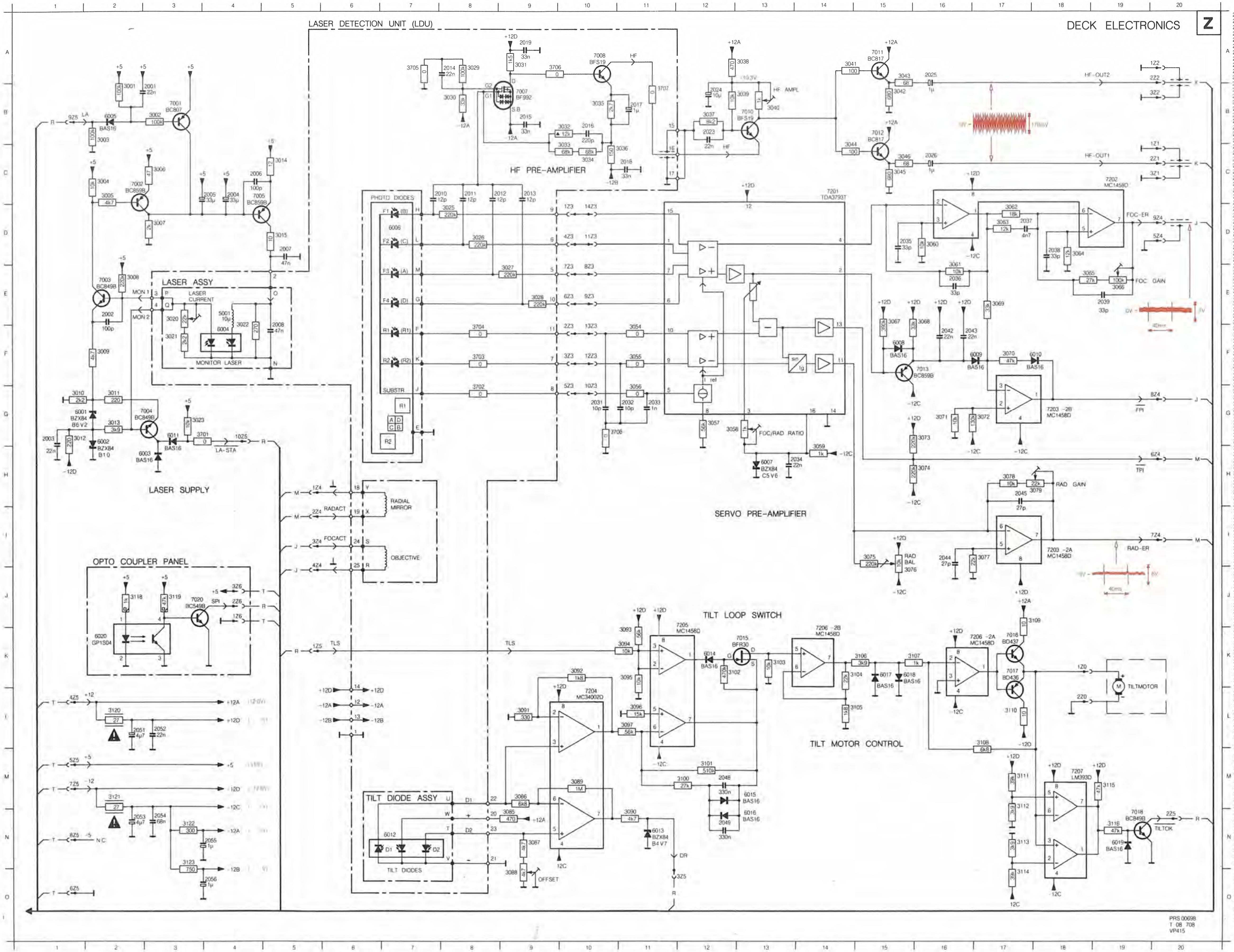
Fuse Resistors

3120	4822 111 30892	27 Ω
3121	4822 111 30892	27 Ω

2001	4822 122 31759	22 nF	
2002	4822 122 32974	100 pF	
2003	4822 122 31759	22 nF	
2004	4822 124 22194	33 µF	10 V
2005	4822 124 22194	33 µF	10 V
2006	4822 122 32974	100 pF	
2007	4822 122 32542	47 nF	
2023	4822 122 31759	22 nF	
2024	4822 124 22193	10 µF	16 V
2025	4822 124 22192	1 µF	16 V
2026	4822 124 22192	1 µF	16 V
2031	4822 122 31971	10 pF	
2032	4822 122 31971	10 pF	
2033	4822 122 32972	1 nF	
2034	4822 122 31759	22 nF	
2035	4822 122 32975	33 pF	
2036	4822 122 32975	33 pF	
2037	4822 122 31784	4.7 nF	
2038	4822 122 32975	33 pF	
2039	4822 122 32975	33 pF	
2042	4822 122 31759	22 nF	
2043	4822 122 31759	22 nF	
2044	4822 122 31966	27 pF	
2045	4822 122 31966	27 pF	
2048	4822 122 33007	330 nF	25 V
2049	4822 122 33007	330 nF	25 V
2051	4822 121 51107	4.7 µF	16 V
2052	4822 122 31759	22 nF	
2053	4822 121 51107	4.7 µF	16 V
2054	4822 122 32891	68 nF	
2055	4822 124 22192	1 µF	16 V
2056	4822 124 22192	1 µF	16 V



PCB.00200
T-08 710



2001	B 3	3123	N 3
2002	E 2	3701	G 4
2003	G 1	3702	G 8
2004	C 4	3703	F 8
2005	C 4	3704	F 8
2006	C 4	3705	A 7
2007	D 5	3706	A 9
2008	E 5	3707	B11
2010	C 8	3708	G11
2011	C 8	5001	E 4
2012	C 9	6001	G 1
2013	C 9	6002	G 2
2014	A 8	6003	H 3
2015	B 9	6004	F 4
2016	B10	6005	B 2
2017	B11	6006	D 7
2018	C11	6007	H13
2019	A 9	6008	F15
2023	B12	6009	F17
2024	B12	6010	F18
2025	A16	6011	G 3
2026	C16	6012	N 7
2031	G10	6013	N11
2032	G11	6014	K12
2033	G11	6015	M13
2034	H14	6016	N13
2035	D15	6017	K15
2036	E16	6018	K15
2037	D17	6019	N19
2038	D18	6020	K 2
2039	E19	7001	B 3
2042	F16	7002	C 2
2043	F17	7003	E 2
2044	I 16	7004	G 3
2045	H17	7005	C 4
2048	M12	7007	B 9
2049	N12	7008	A10
2051	L 2	7010	B13
2052	L 3	7011	A15
2053	N 2	7012	B15
2054	N 3	7013	F16
2055	N 4	7015	K13
2056	O 4	7016	K17
3001	B 2	7017	K17
3002	B 3	7018	N19
3003	B 2	7020	J 3
3004	C 2	7201	C14
3005	C 2	7202	C19
3006	C 3	7203	G18
3007	D 3	7203	I 18
3008	E 2	7204	L10
3009	F 2	7205	J12
3010	G 1	7206	K14
3011	G 2	7206	K17
3012	G 1	7207	M18
3013	G 2		
3014	C 5		
3015	D 5		
3020	E 3		
3021	F 3		
3022	E 4		
3023	G 3		
3025	D 8		
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3028	E 9		
3029	A 8		
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3079	H18		
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3088	O 9		
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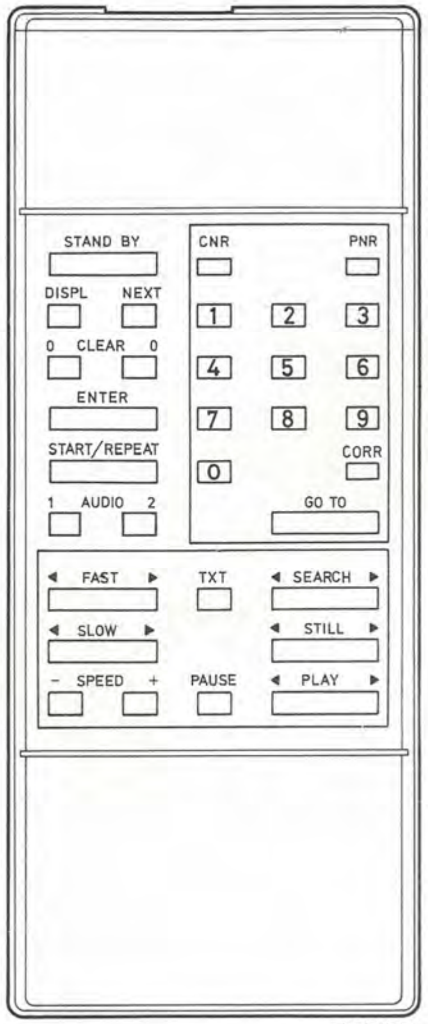
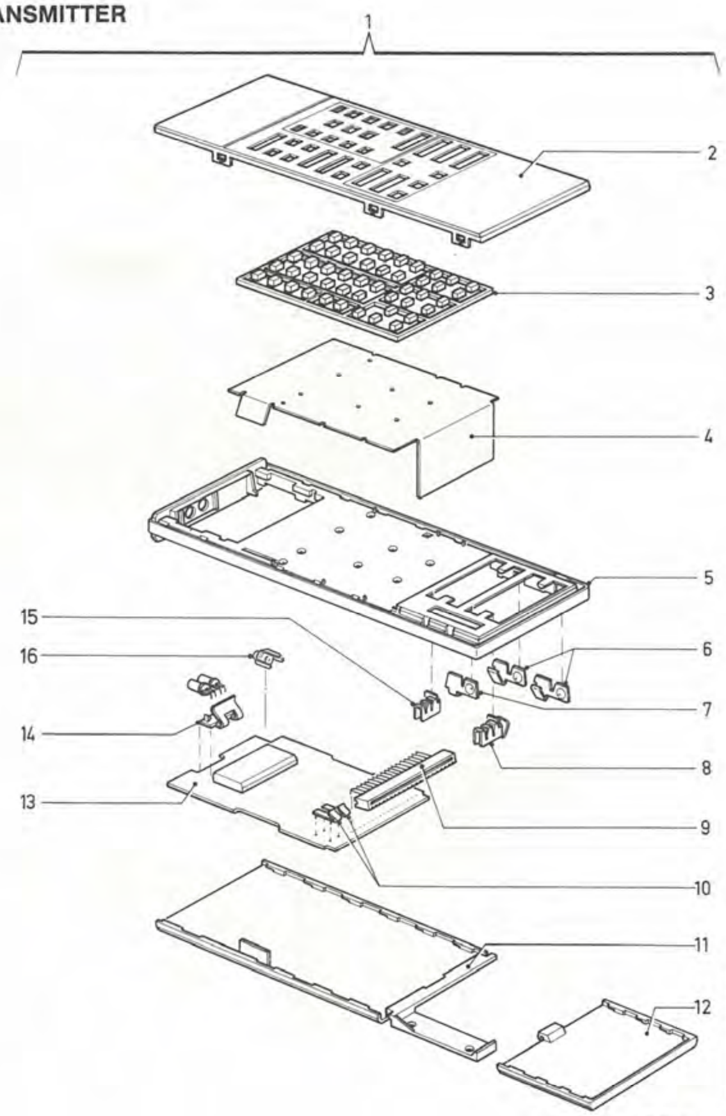
3103	K13		
3104	K15		
3105	L15		
3106	K15		
3107	K16		
3108	L17		
3109	J18		
3110	L17		
3111	M17		
3112	M17		
3113	N17		
3114	O17		
3115	M19		
3116	N19		
3118	J 2		
3119	J 3		
3120	L 2		
3121	M 2		
3122	N 3		

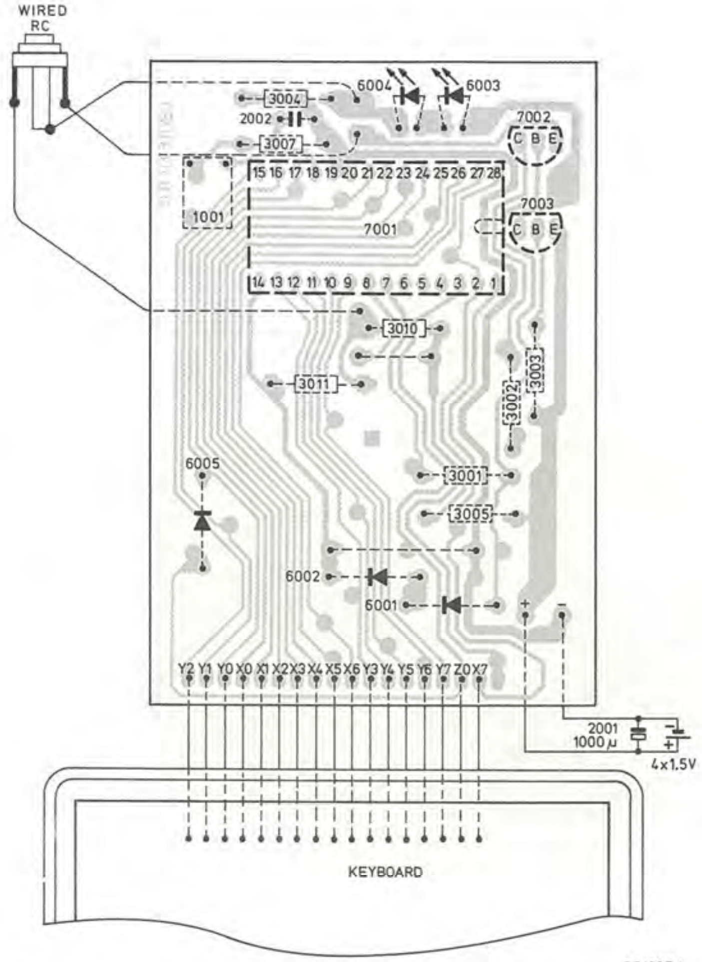
REMOTE CONTROL RC53/VP410/VP415 TRANSMITTER



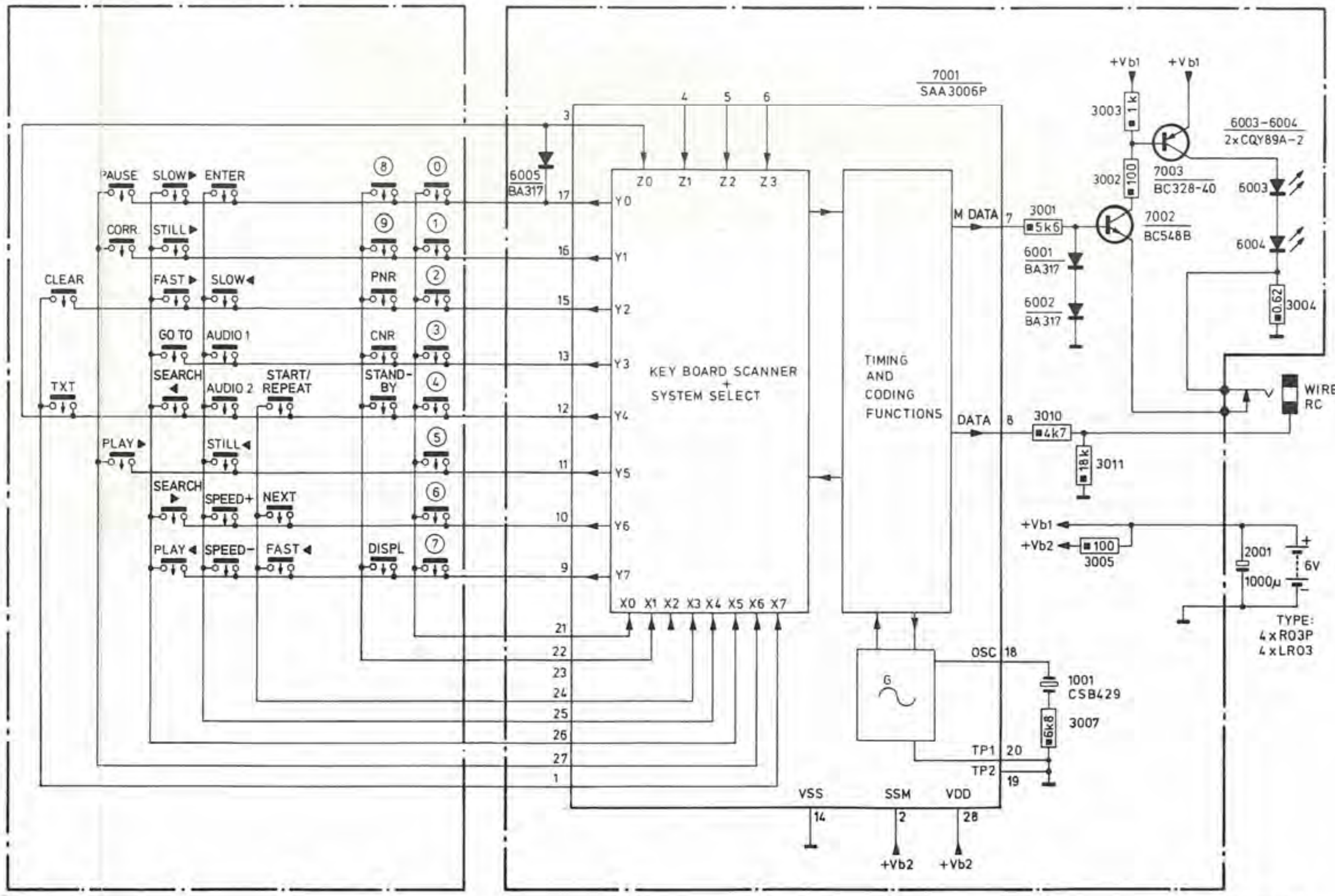
39 865 B12



39 863 C12



35188B4



39 864 C12

ELECTRICAL PARTS

Batteries
4x R03P 1.5V

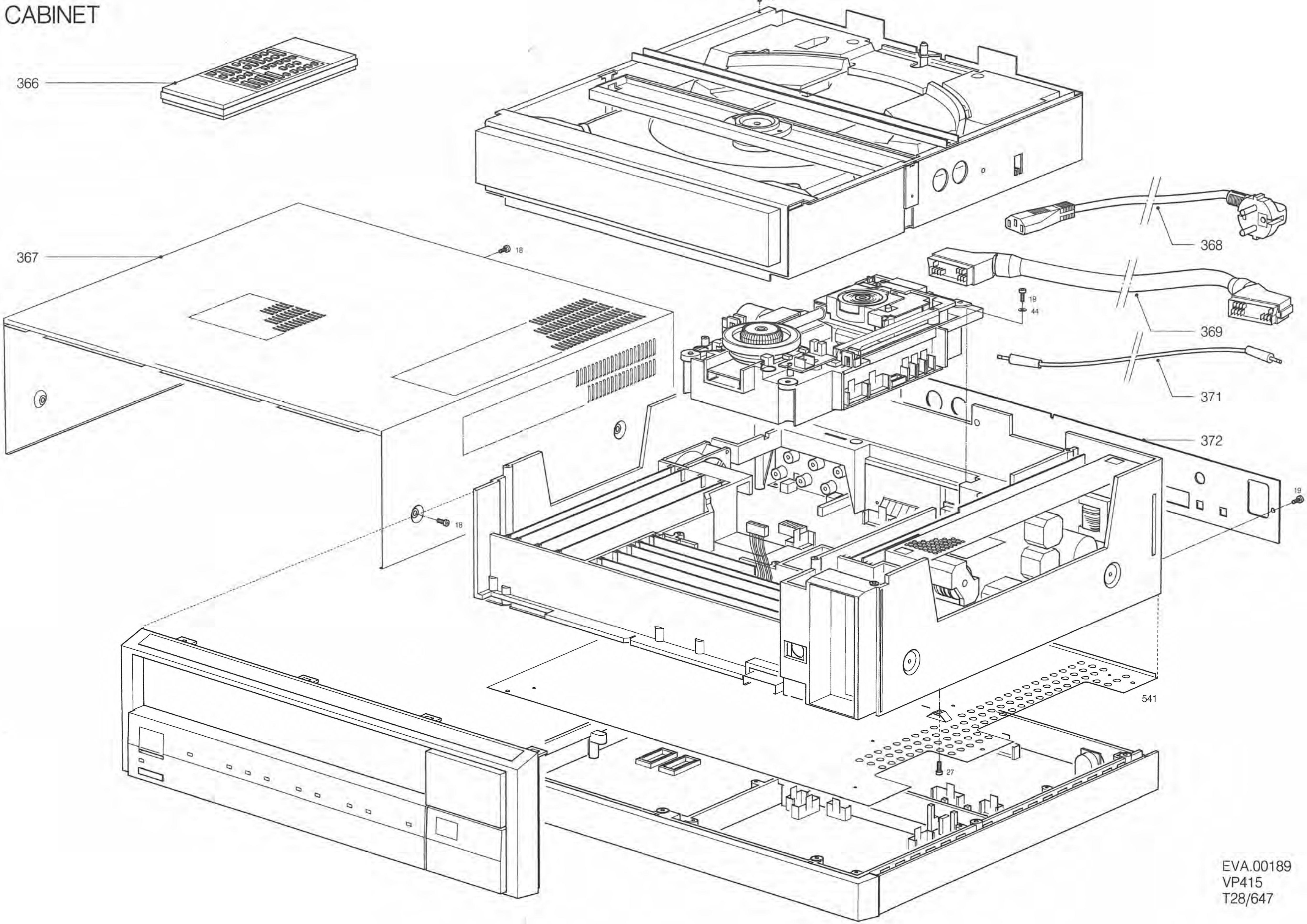
Crystals		
1001	4822 242 71498	CSB429
Integrated circuits		
7001	4822 209 81891	SAA3006P
Transistors		
7002	4822 130 40937	BC548B
7003	4822 130 41715	BC328–40
LEDs		
6003	4822 130 31332	CQY89A–2
6004	4822 130 31332	CQY89A–2
Diodes		
6005	4822 130 30847	BA317
Capacitors		
2001	4822 124 21341	1000 μF 8V
Resistors		
3004	4822 110 73027	0.62 Ω

MECHANICAL PARTS

1	4822 218 20607	Transmitter complete
2	4822 432 30284	Top cover
3	4822 410 25423	Knob assembly
4	4822 276 80313	Switch panel
5	4822 432 30283	Casing
6	4822 492 62879	Battery contact
7	4822 492 62881	Battery contact
8	4822 492 62883	Battery contact
9	4822 267 50418	Connector
10	4822 492 62904	Spring
11	4822 432 30282	Bottom
12	4822 432 30281	Battery lid
13	4822 214 50358	Printed board
14	4822 256 90506	LED holder
15	4822 492 62882	Battery contact
16	4822 267 50443	Connector

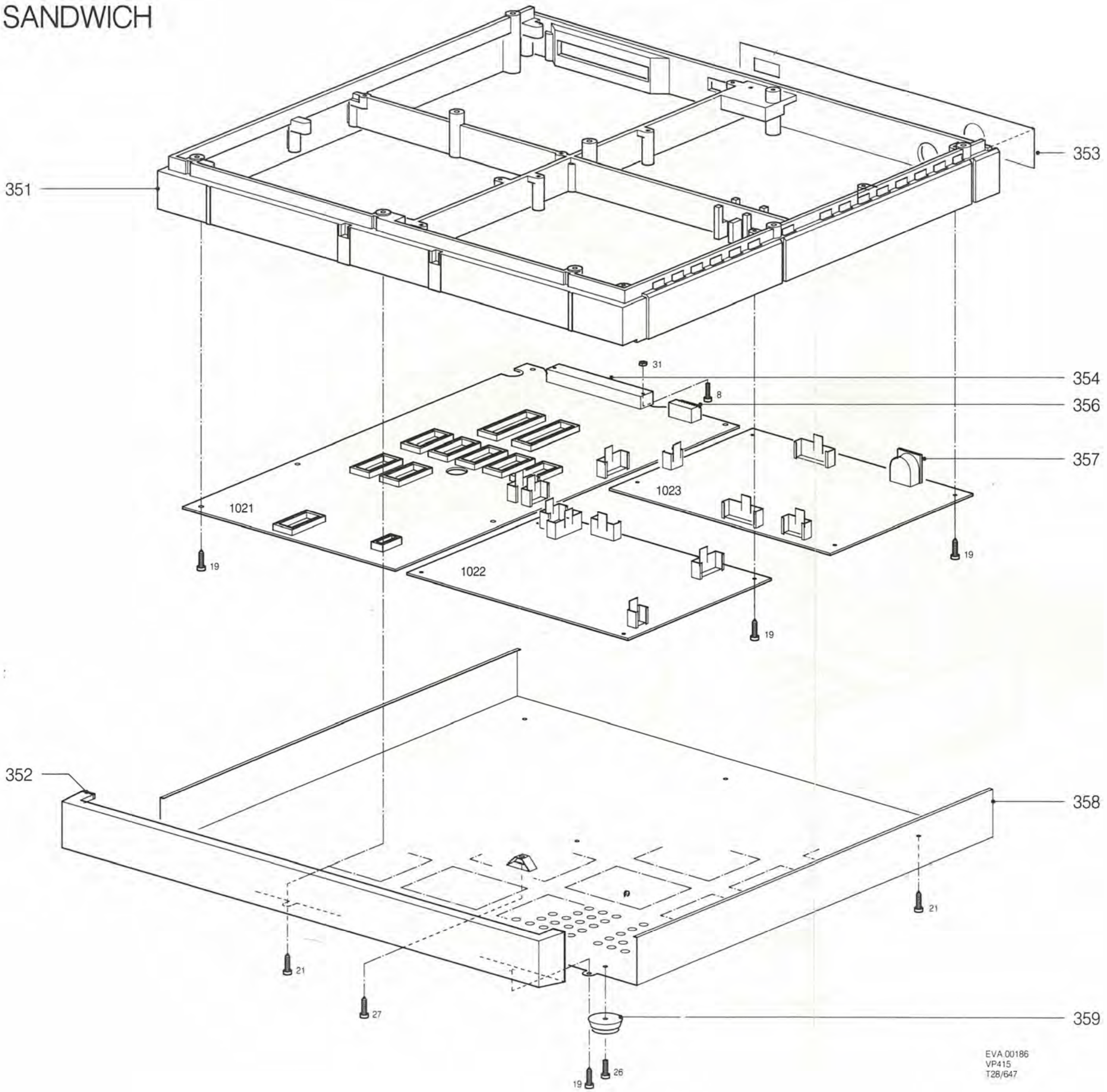
Exploded view drawings
List of mechanical parts
List of electrical parts

CABINET



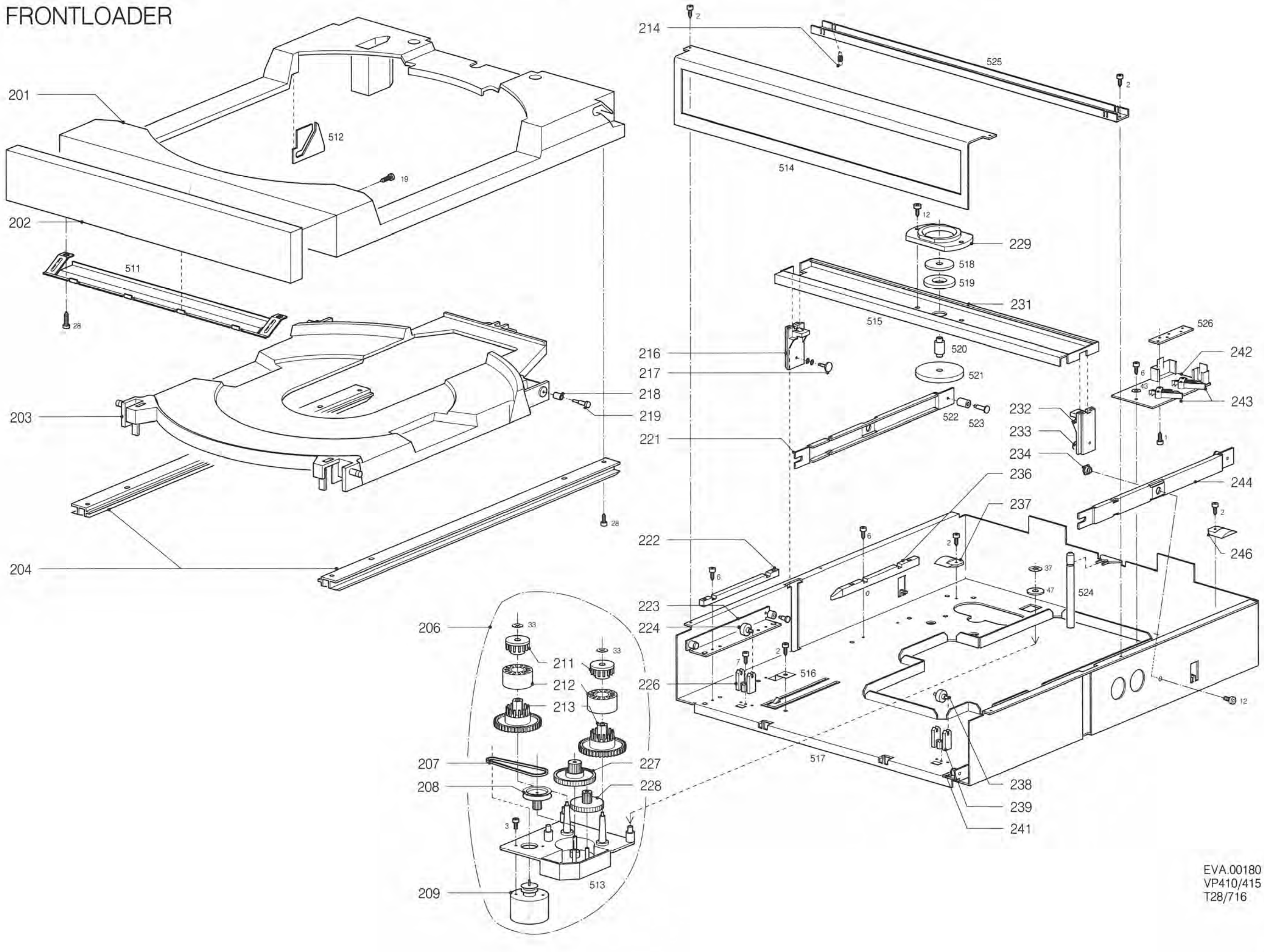
EVA.00189
VP415
T28/647

SANDWICH



351
353
354
356
357
31
8
1021
1022
1023
19
352
358
359
21
27
26
EVA 00186
VP415
T28/647

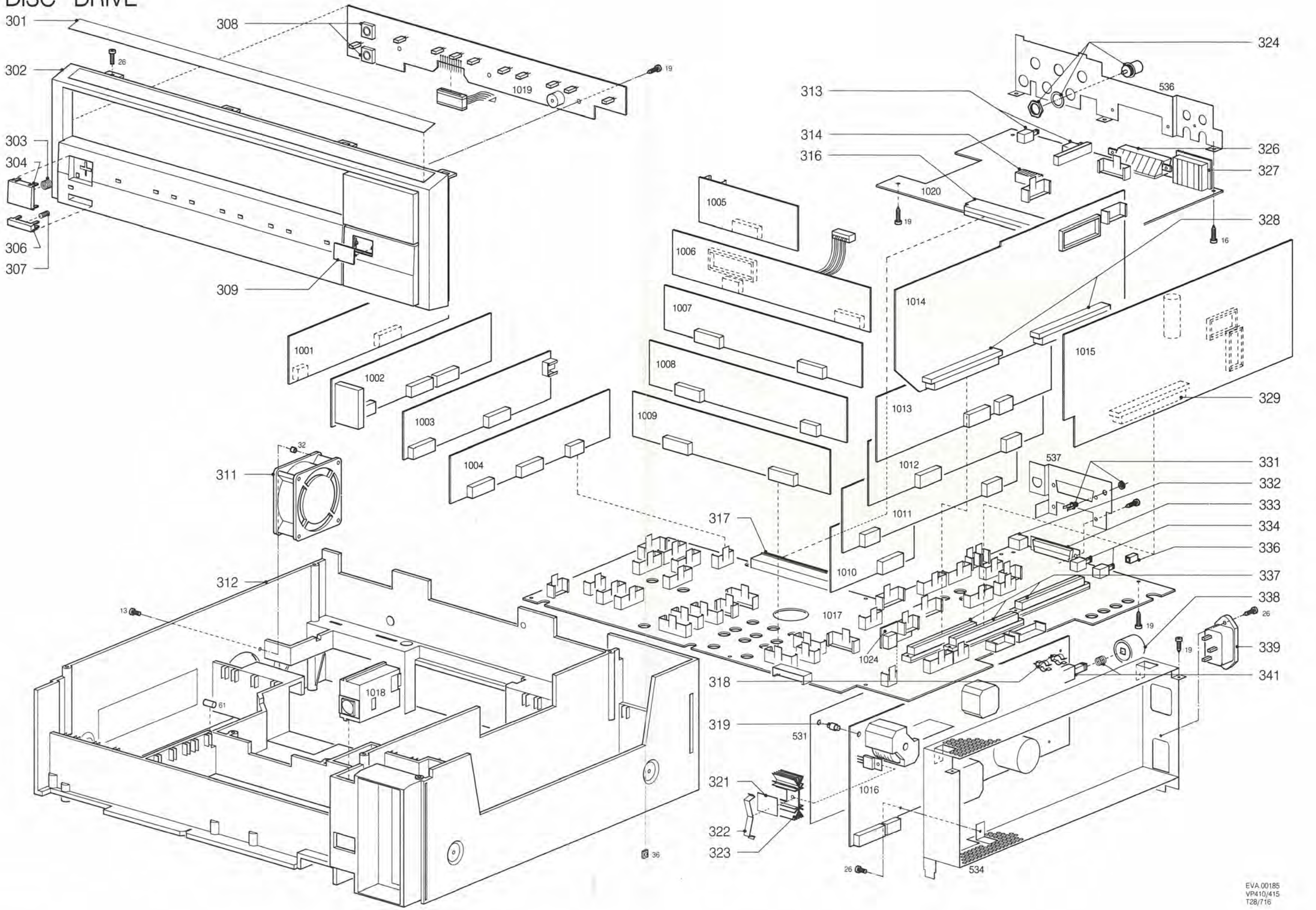
FRONTLOADER



EVA.00180
VP410/415
T28/716

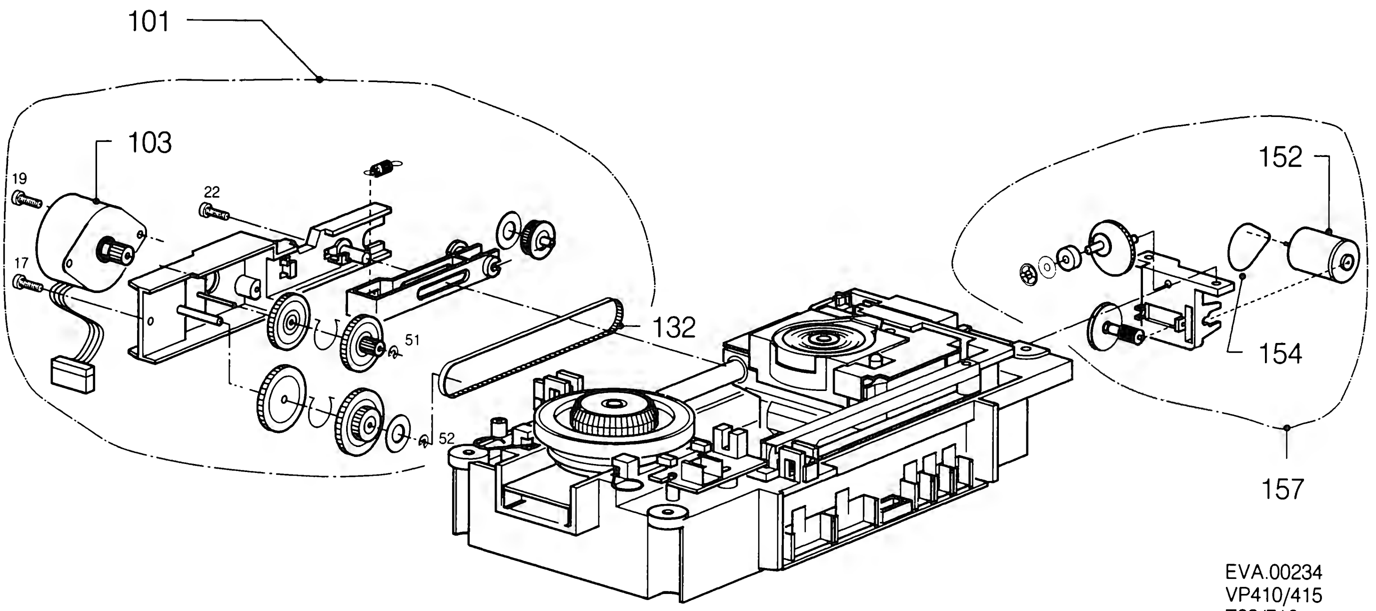
CS 7 865

DISC DRIVE



CS 7 866

OPTICAL DECK



* For differences see item 301 and item 368

LIST OF MECHANICAL PARTS

FIXING MATERIALS

Item	Service codenr	Description
1	4822 502 12555	Screw M 2 x 10
2	4822 502 12797	Screw M 2.5 x 4
3	4822 502 11715	Screw M 2.5 x 5
4	4822 502 12795	Screw M 2.5 x 6
6	4822 502 12798	Screw M 2.5 x 6
7	4822 502 12799	Screw M 2.5 x 8
8	4822 502 11549	Screw M 2.5 x 10
9	4822 502 12796	Screw M 2.5 x 12
11	4822 502 12794	Screw M 3 x 5
12	4822 502 11667	Screw M 3 x 6
13	4822 502 11678	Screw M 3 x 8
14	4822 502 11679	Screw M 3 x 16
16	4822 502 30438	Screw 3 M x 6
17	4822 502 30439	Screw 3 M x 8
18	4822 502 12863	Screw 3 M x 8
19	4822 502 30408	Screw 3 M x 10
21	4822 502 30409	Screw 3 M x 12
22	4822 502 30412	Screw 3 M x 20
24	4822 502 30331	Screw 2 N x 6.5
26	4822 502 30303	Screw 4 N x 6.5
27	4822 502 30085	Screw 4 N x 9.5
28	4822 502 30314	Screw 4 N x 22
31	4822 505 10888	Nut M 2.5 Hex nut
32	4822 505 10891	Nut M 3 Press in nut
33	4822 505 10892	Nut M 3 Speed nut
34	4822 505 10717	Nut M 3 Hex nut
36	4822 505 10635	Nut M 3 Lock nut
37	4822 505 10893	Nut M 4 Speed nut
41	4822 532 10215	Washer 2.7 x 6
43	4822 532 10332	Washer 3.2 x 7
44	4822 532 51843	Washer 3.2 x 9
47	4822 532 51844	Washer
51	4822 530 70121	Retaining ring 1.5
52	4822 530 70122	Retaining ring 1.9
53	4822 530 70043	Retaining ring 2.3
61	4822 462 40155	Stopper

OPTICAL DECK

101	4822 691 30185	Slide drive assy
103	4822 361 20963	Motor assy
132	4822 358 20264	Toothbelt
152	4822 361 20964	ATC Motor assy
154	4822 358 10107	Belt
157	4822 691 30186	ATC drive assy

FRONTLOADER

201	4822 418 40547	Tray assy
202	4822 691 30184	Front tray assy
203	4822 532 61051	Disc carrier
204	4822 466 82136	Guide section
206	4822 691 20403	Frontloading drive
207	4822 358 30741	Belt
208	4822 528 81143	Pulley
209	4822 361 20933	Motor assy
211	4822 532 61049	Mounting bush
212	4822 528 90636	Friction wheel
213	4822 522 32254	Gear wheel
214	4822 492 32671	Tension spring
216	4822 466 82139	Slide block
217	4822 535 92288	Pin
218	4822 528 90637	Roller
219	4822 535 92289	Pin
221	4822 402 61074	Bracket assy
222	4822 402 61075	Guide support
223	4822 402 61072	Guide bracket
224	4822 528 90634	Wheel
226	4822 466 82137	Block
227	4822 522 32253	Gear wheel
228	4822 522 32252	Gear wheel
229	4822 532 51845	Catch ring
231	4822 402 61073	Pressure bracket assy
232	4822 466 82139	Slide block
233	4822 535 92288	Pin
234	4822 528 90635	Nave
236	4822 466 82138	Guide support
237	4822 528 30324	Rise cam
238	4822 528 90634	Wheel
239	4822 466 82137	Block
241	4822 402 61072	Guide bracket
242	4822 214 51583	Printed board assy
243	4822 276 11897	Switch assy
244	4822 402 61074	Bracket assy
246	4822 528 30324	Rise cam

DISC DRIVE

301	4822 454 30372	Ornamental plate (/00/35)
301	4822 454 30357	Ornamental plate (/05)
302	4822 444 40157	Front assy
303	4822 492 51891	Spring
304	4822 410 25447	Eject knob
306	4822 410 25448	Stand by knob
307	4822 492 51889	Spring
308	4822 276 10974	Switch
309	4822 381 10846	Window R.C.
311	4822 361 10443	Fan assy
312	4822 464 50639	Frame assy
313	4822 276 11301	Switch
314	5322 277 20916	Dip switch
316	4822 267 40701	Connector 64p
317	4822 267 70203	Connector 64p
318	4822 492 63671	Fuse holder spring
319	5322 256 90712	Spacer
321	5322 466 70555	Insulating plate
322	4822 402 61083	Clamping spring
323	4822 255 40778	Heat sink
324	4822 267 10161	BNC connector
326	4822 267 60198	SCART connector
327	4822 267 40586	Cinch connector
328	4822 267 40701	Connector
329	4822 267 40701	Connector
331	4822 267 50443	Connector
332	4822 271 30575	Dip switch
333	4822 267 60161	Connector
334	4822 276 11301	Switch
336	4822 410 23697	Knob
337	4822 267 70202	Connector
338	4822 410 22364	Knob
339	4822 265 30299	Connector
341	4822 276 12035	Mainsswitch

SANDWICH

351	4822 464 50641	Frame assy
352	4822 444 40158	Front
353	4822 454 30359	Textplate
354	5322 265 61077	Connector 50p
356	4822 271 30576	Dip switch
357	4822 267 40284	Socket
358	4822 443 61966	Cover
359	4822 462 71261	Foot

CABINET

366	4822 218 20607	R.C. Transmitter
367	4822 444 60462	Cover assy
368	4822 321 10497	Mainscord (/00)
368	4822 321 10472	Mainscord (/05/35)
369	4822 321 20486	SCART cable
371	4822 321 22236	R.C. cord
372	4822 454 30358	Textplate assy

IC SOCKETS

5322 255 44122	14p.
5322 255 44047	28p.
5322 255 44217	40p.

CONNECTORS

male top

4822 267 40352	3p.
4822 267 40353	4p.
4822 267 40354	5p.
4822 267 40355	6p.
4822 267 50285	7p.
4822 267 50406	8p.
4822 265 40229	9p.
4822 267 50332	10p.

male side

4822 267 50719	3p.
4822 267 40685	3p.
4822 267 40702	6p.
4822 267 50694	8p.
4822 267 50691	9p.
4822 267 50692	10p.
4822 267 50695	10p.
4822 267 50693	12p.
4822 267 50696	12p.

MODULE CONNECTORS

male (on module carrier)

4822 267 50591	6p.
4822 264 50149	10p.

female (on moduie)

4822 265 40469	6p.
4822 265 40472	10p.

LIST OF ELECTRICAL PARTS

R.C.–T	4822 218 20607	Remote control transmitter
R.C.–R	4822 212 21449	Remote control receiver

INTEGRATED CIRCUITS

4822 209 71276	CLX1004
4822 209 71275	CLX5001
4822 209 71274	GSCXB38113P01
4822 209 10246	HEF4001BP
4822 209 10247	HEF4011BP
4822 209 10294	HEF4012BP
4822 209 10248	HEF4013BP
4822 209 10249	HEF4015BP
5322 209 14119	HEF4016BP
5322 209 10344	HEF40161BP
5322 209 11295	HEF40163BP
4822 209 10284	HEF40175BP
5322 209 84508	HEF4022BP
4822 209 11425	HEF40240BP
5322 209 10489	HEF40244BP
5322 209 10867	HEF40245BP
4822 209 10301	HEF4028BP
4822 209 10302	HEF4029BP
5322 209 14124	HEF4030BP
5322 209 10385	HEF40374BP
4822 209 10303	HEF4041BP
4822 209 10306	HEF4049BP
5322 209 10576	HEF4053BP
5322 209 10357	HEF4066BP
4822 209 10322	HEF4068BP
4822 209 10307	HEF4071BP
4822 209 10269	HEF4081BP
5322 209 14927	HEF4093BP
5322 209 10421	HEF4094BP
4822 209 10273	HEF4104BP
4822 209 10866	HEF4528BP
4822 209 10291	HEF4538BP
4822 209 10313	HEF4539BP
4822 209 10279	HEF4555BP
5322 209 10473	HEF4557BP
5322 209 85503	LM311N
4822 209 71285	LM358
5322 209 70225	LM393D
4822 209 80797	LM393N
4822 209 71279	LM4921
4822 209 10948	MAB8031AH–12P
4822 209 71278	MB88303
4822 209 10247	MC14011BCP
5322 209 10576	MC14053BCP
4822 209 70434	MC14094BCP
4822 209 81091	MC14538BCP
4822 209 71469	MC1458D
4822 209 81349	MC1458P1
5322 209 84307	MC1488P
4822 209 71309	MC1489AP
4822 209 80617	MC1741CP1
4822 209 71382	MC34002BP
4822 209 71361	MC34002P
4822 209 11345	MC78L08ACP
4822 209 10379	MSM2128–20RS
4822 209 71273	NCR5385E
5322 209 86546	NE527N
5322 209 86234	NE5532N
4822 209 81132	NE5535N
5322 209 85311	N74LS32N
5322 209 82215	N74LS245N
5322 209 86258	N74LS377N
4822 209 71381	PA0017
4822 209 11431	PCF0706P/008
5322 209 11106	PC74HCT02P
4822 209 82341	PC74HCT04P
4822 209 11427	PC74HCT11P
5322 209 11266	PC74HCT32P
5322 209 82575	PC74HCT74P
4822 209 11426	PC74HCT86P
4822 209 83044	PC74HCT132P
4822 209 11429	PC74HCT153P
4822 209 11428	PC74HCT4075P
4822 209 71277	PD0011
5322 209 81468	SAA1043P
4822 209 80823	SAA1061
4822 209 82786	SAA5230/V2
4822 209 11327	SAA7000/0704
4822 209 10857	SAA7010
4822 209 10377	SAA7020
4822 209 80641	SN74LS00N
4822 209 80783	SN74LS04N
5322 209 81626	SN74LS08N
4822 209 71281	SN74LS26N
5322 209 85311	SN74LS32N
4822 209 71283	SN74LS38N
4822 209 80782	SN74LS74AN
4822 209 71282	SN74LS76AN
5322 209 85266	SN74LS123N
5322 209 85647	SN74LS138N
5322 209 85752	SN74LS155N
5322 209 85862	SN74LS240N
5322 209 86017	SN74LS244N
5322 209 86062	SN74LS373N
5322 209 81646	SN74LS374N
5322 209 85938	SN74LS670N
4822 209 80629	TCA240
4822 209 81062	TDA1432P
4822 209 82146	TDA2501
4822 209 83227	TDA2595/V5
4822 209 80744	TDA2730
4822 209 83272	TDA3505/V7
4822 209 71319	TDA3793T
4822 209 83273	TDA4555
4822 209 71284	TDA4560
4822 209 71311	TL431CLP
4822 209 11412	TL8704P
*4822 209 71312	TMS27128–20JL
*4822 209 71317	TMS27512–20JL
4822 209 71316	UAA1031
4822 209 71315	UA78L06ACLP
5322 130 44843	UA7905UC
4822 209 11438	UPD4364C–20L
4822 209 10914	UPD8041AHC–152
4822 209 71314	UPD8155C–2
4822 209 71313	UPD8255A–5
5322 209 10179	Z8400A

* = not programmed

TRANSISTORS

5322 130 44476	BC264A
4822 130 41066	BC264B
5322 130 44476	BC264C
5322 130 44656	BC264D
4822 130 40854	BC327
4822 130 41246	BC327−25
4822 130 41327	BC327−40
5322 130 44647	BC368
5322 130 44593	BC369
4822 130 60491	BC375
4822 130 60492	BC376
4822 130 44461	BC546B
4822 130 40959	BC547B
4822 130 40937	BC548B
4822 130 40936	BC549B
4822 130 41691	BC556B
4822 130 44256	BC557
4822 130 44197	BC558B
4822 130 41053	BC639
4822 130 41078	BC640
4822 130 42132	BC807
4822 130 42133	BC817
4822 130 42804	BC817−25
4822 130 60511	BC847B
5322 130 41982	BC848B
5322 130 42136	BC848C
4822 130 60512	BC849
4822 130 42711	BC849B
5322 130 41983	BC858B
4822 130 60513	BC859
4822 130 60514	BC859B
4822 130 60516	BC859C
4822 130 40823	BD135
4822 130 40995	BD434
5322 130 50405	BD435
4822 130 60089	BD436
4822 130 40982	BD437
4822 130 40995	BD438
5322 130 44418	BF256A
5322 130 44744	BF256B
4822 130 44237	BF450
4822 130 44195	BF494
4822 130 41376	BF494B
4822 130 60515	BF992
5322 130 44343	BFR30
4822 130 41801	BFR54
4822 130 42353	BFS19
4822 130 60517	BSD213
5322 130 44093	BSV78
5322 130 34044	BSV80
5322 130 44788	BSW68A
4822 130 60518	BU406F
4822 130 42678	BUT11F
5322 130 42492	BUW12
4822 130 60509	BUW85
5322 130 44718	BUX86
4822 130 41594	PH2369

DIODES

4822 130 30621	1N4148
4822 130 30847	BA317
5322 130 31928	BAS16
4822 130 31983	BAT85
4822 130 30842	BAV21
4822 130 30613	BAW62
5322 130 33756	BAX12
4822 130 34121	BAX18
4822 130 32227	BB112
4822 130 31129	BB212
5322 130 31684	BB809
4822 130 20091	BT151−800R
5322 130 34761	BY224−600
4822 130 80112	BYR29−600
5322 130 32184	BYV27−50
4822 130 31982	BYV27−100
4822 130 32213	BYV28−50
5322 130 31637	BYV32−150
5322 130 32039	BYV33−40
5322 130 32246	BYV33−45
5322 130 34979	BYV96E
4822 130 31347	BYW96D
5322 130 32172	BZT03−C110
4822 130 31248	BZV46−C2V0
4822 130 34047	BZX75−C1V4
4822 130 34049	BZX75−C2V1
4822 130 34048	BZX75−C2V8
4822 130 34167	BZX79−B6V2
4822 130 31024	BZX79−B18
5322 130 31504	BZX79−C3V3
4822 130 34233	BZX79−C5V1
4822 130 34167	BZX79−C6V2
4822 130 34258	BZX79−C56
4822 130 33707	BZX84−B6V2
4822 130 33698	BZX84−B10
5322 130 31937	BZX84−C4V7
4822 130 80125	BZX84−C5V6
5322 130 33671	BZX84−C6V2
4822 130 33294	BZX84−C8V2
4822 130 33996	BZX84−C9V1
4822 130 32565	HZ3C2(3V3)
4822 130 80114	HZ4A2(3V6)
4822 130 32843	HZ4B2(3V9)
4822 130 80109	HZ4C3(4V3)
4822 130 32986	HZ5B1(4V7)
4822 130 33293	HZ5C2(5V1)
4822 130 32697	HZ6A3(5V6)
4822 130 32698	HZ6C2(6V2)
4822 130 33523	HZ7A3(6V8)
4822 130 32862	HZ7C2(7V5)
4822 130 33294	HZ9A2(8V2)
4822 209 70289	HZ9C1(9V1)
4822 130 32566	HZ11A3(10V0)
4822 209 71575	HZ11C1(11V0)

STANDARD RESISTORS

MR25 Resistors

5322 116 55483	10 Ω
5322 116 54459	75 Ω
5322 116 54497	226 Ω
5322 116 50592	442 Ω
4822 116 51235	1 kΩ
5322 116 53321	1.27 kΩ
5322 116 54004	2.43 kΩ
5322 116 50671	2.61 kΩ
5322 116 55445	4.87 kΩ
5322 116 54606	7.15 kΩ
5322 116 51253	10 kΩ

MRS25 Resistors

4822 116 52891	10 Ω
5322 116 54964	31.6 Ω
4822 116 53056	68 Ω
5322 116 53264	68.1 Ω
5322 116 53339	75 Ω
4822 116 53794	120 Ω
4822 116 52846	150 Ω
5322 116 53259	237 Ω
4822 116 53496	390 Ω
4822 116 53423	470 Ω
4822 116 53108	1 kΩ
5322 116 53257	1.62kΩ
5322 116 53605	2 kΩ
5322 116 53551	3.9 kΩ
4822 116 53027	5.6 kΩ
4822 116 53022	10 kΩ
4822 116 53081	12 kΩ
5322 116 53235	17.8 kΩ
4822 116 53084	18 kΩ
5322 116 53241	21.5 kΩ
5322 116 53262	31.6 kΩ
4822 116 52856	43 kΩ
4822 116 52857	47 kΩ
5322 116 53266	75 kΩ
4822 116 52973	100 kΩ
5322 116 53256	147 kΩ
4822 116 52843	1 MΩ

Chip Resistors

4822 111 90163	0 Ω
5322 111 90104	2.2 Ω
4822 111 90391	3.9 Ω
5322 111 90376	4.7 Ω
5322 111 90095	10 Ω
4822 111 90341	12 Ω
4822 111 90344	15 Ω
4822 111 90186	22 Ω
4822 116 60172	27 Ω
4822 111 90357	33 Ω
4822 111 90361	39 Ω
4822 111 90217	47 Ω
4822 111 90203	68 Ω
5322 111 90091	100 Ω
4822 111 90339	120 Ω
4822 116 60164	130 Ω
5322 111 90098	150 Ω
5322 111 90242	180 Ω
4822 116 52849	200 Ω
4822 111 90178	220 Ω
4822 111 90353	240 Ω
4822 111 90154	270 Ω
4822 111 90156	300 Ω
5322 111 90106	330 Ω

Chip Resistors

5322 111 90138	390 Ω
5322 111 90109	470 Ω
4822 111 90245	510 Ω
5322 111 90113	560 Ω
4822 111 90805	620 Ω
4822 111 90162	680 Ω
4822 111 90438	750 Ω
4822 111 90171	820 Ω
5322 111 90092	1 kΩ
5322 111 90096	1.2 kΩ
4822 111 90244	1.3 kΩ
4822 111 90151	1.5 kΩ
5322 111 90101	1.8 kΩ
4822 116 60167	2 kΩ
4822 111 90248	2.2 kΩ
4822 111 90289	2.4 kΩ
4822 111 90569	2.7 kΩ
4822 111 90157	3.3 kΩ
5322 116 53738	3.6 kΩ
4822 116 60156	3.9 kΩ
5322 111 90111	4.7 kΩ
5322 111 90268	5.1 kΩ
4822 111 90572	5.6 kΩ
4822 111 90545	6.2 kΩ
4822 111 90544	6.8 kΩ
5322 111 90118	8.2 kΩ
4822 111 90373	9.1 kΩ
4822 111 90249	10 kΩ
4822 111 90337	11 kΩ
4822 111 90253	12 kΩ
4822 111 90509	13 kΩ
4822 111 90196	15 kΩ
4822 111 90238	18 kΩ
4822 111 90251	22 kΩ
4822 111 90542	27 kΩ
5322 111 90267	33 kΩ
4822 111 90514	36 kΩ
5322 111 90108	39 kΩ
4822 111 90543	47 kΩ
4822 111 90573	56 kΩ
4822 111 90202	68 kΩ
4822 111 90574	75 kΩ
4822 116 60185	82 kΩ
4822 111 90214	100 kΩ
4822 116 52844	110 kΩ
4822 111 90568	120 kΩ
4822 111 90511	130 kΩ
4822 116 60166	150 kΩ
4822 111 90565	180 kΩ
4822 111 90197	220 kΩ
4822 111 90215	240 kΩ
4822 111 90302	270 kΩ
4822 116 53801	300 kΩ
4822 111 90513	330 kΩ
4822 111 90182	390 kΩ
4822 111 90161	470 kΩ
4822 111 90364	510 kΩ
4822 111 90169	560 kΩ
4822 111 90368	680 kΩ
4822 111 90205	820 kΩ
5322 111 91141	1 MΩ
4822 111 90409	1.2 MΩ
4822 111 90429	1.5 MΩ
4822 111 90191	1.8 MΩ
4822 111 90237	8.2 MΩ

Chapter 6

LaserVision ROM disc drive VP415/00/05/35

Service
Service
Service

LaserVision


42 050 A12

Repair Method

Contents:

Published by
Service Consumer Electronics

CS 8 110

Repair Method VP415

1. Introduction

The object of this repair method is to facilitate faultfinding in a defective set for the service technician. The method is set up in such a way that the fault diagnosis in a set under repair is made via a test procedure. In this test procedure several operations should be carried out sequentially and decisions should be made on various points. Via a yes/no decision, the technician is led to a defective module or part of it. A central role in the repair method is played by the Diagnostic Software, which has been implemented in the Drive Processor.

2. Diagnostic Software

In the control of the various functions in the set, an important role is played by Drive Processor module R. For this reason the diagnostic software forms an integral part of the drive software of this module.

a. *Set–up*

The diagnostic software has been integrated in the drive software in such a way that many of the tasks of the drive are checked for proper performance. If a fault is detected in the execution of a task, an error code is shown on the screen as video overlay.
The error code meets the following priority rule:

1 – 30 fatal fault
31 – 59 major fault
60 – 80 behaviour fault
81 – 99 minor fault
100 – 254 for development
255 initial value (Display – – –)

The lower the error code, the more serious the fault.

b. *Switching on the Diagnostic Software*

A fault can be detected in two different modes:

1. **Check mode**
The error code is shown on the screen during manual– or computercontrolled use.
You can enable this check mode by switching on the mains switch while keeping the STAND–BY key on the front panel depressed. Do not release the STAND–BY key until 3 horizontal stripes are visible in the right–hand bottom corner of the picture screen.

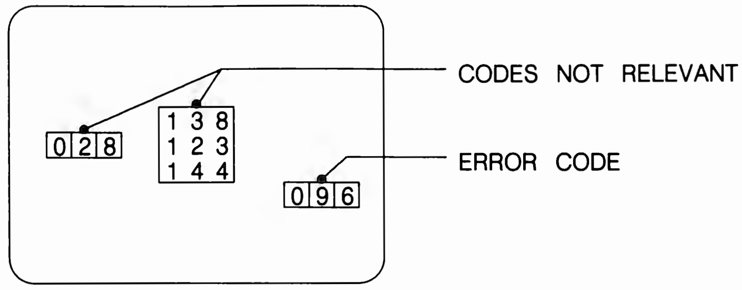
2. **Self–test mode**
Now the drive is controlled in a programme loop while the normal operating functions are inoperative.
You can enable the self–test mode by pressing the mains switch while keeping both the EJECT and the STAND–BY key depressed. Do not release the two keys until the word DIAGNOSTICS appears on the screen.
Now the screen not only shows the error code, but also the position of the loop counter and the text DIAGNOSTICS.
The occurrence of minor faults (error code > 60) does not influence the execution of the programme loops; on the other hand, faults having an error code < 60 will interrupt the programme loop and switch the drive into position STAND–BY while keeping the last LDU–slide position.

Both modes are reset again after the mains switch is switched off.
It is advisable to switch off the set only when it is in STAND–BY mode.

c. *Reproducing the error codes on the screen*

The error code is shown as video overlay on the screen as follows:

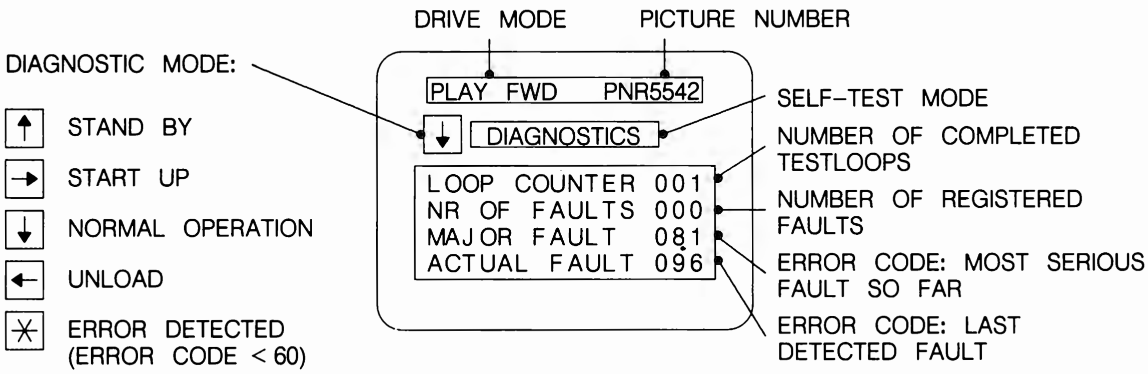
1. **Check mode**



CHECK MODE

The error code is shown in the right-hand bottom corner of the screen.
This is the last detected fault.

2. **Self-test mode**



SELF-TEST MODE

By displaying the text DIAGNOSTICS, the screen indicates that the set is in self-test mode. It also shows the drive mode and the diagnostic mode. In the middle of the screen the position of the loop counter and the number of registered faults are given.
The error codes are divided into major and actual faults.
The code for a major fault shown on the screen will only be overwritten if the new code has priority (that is, a lower error code).

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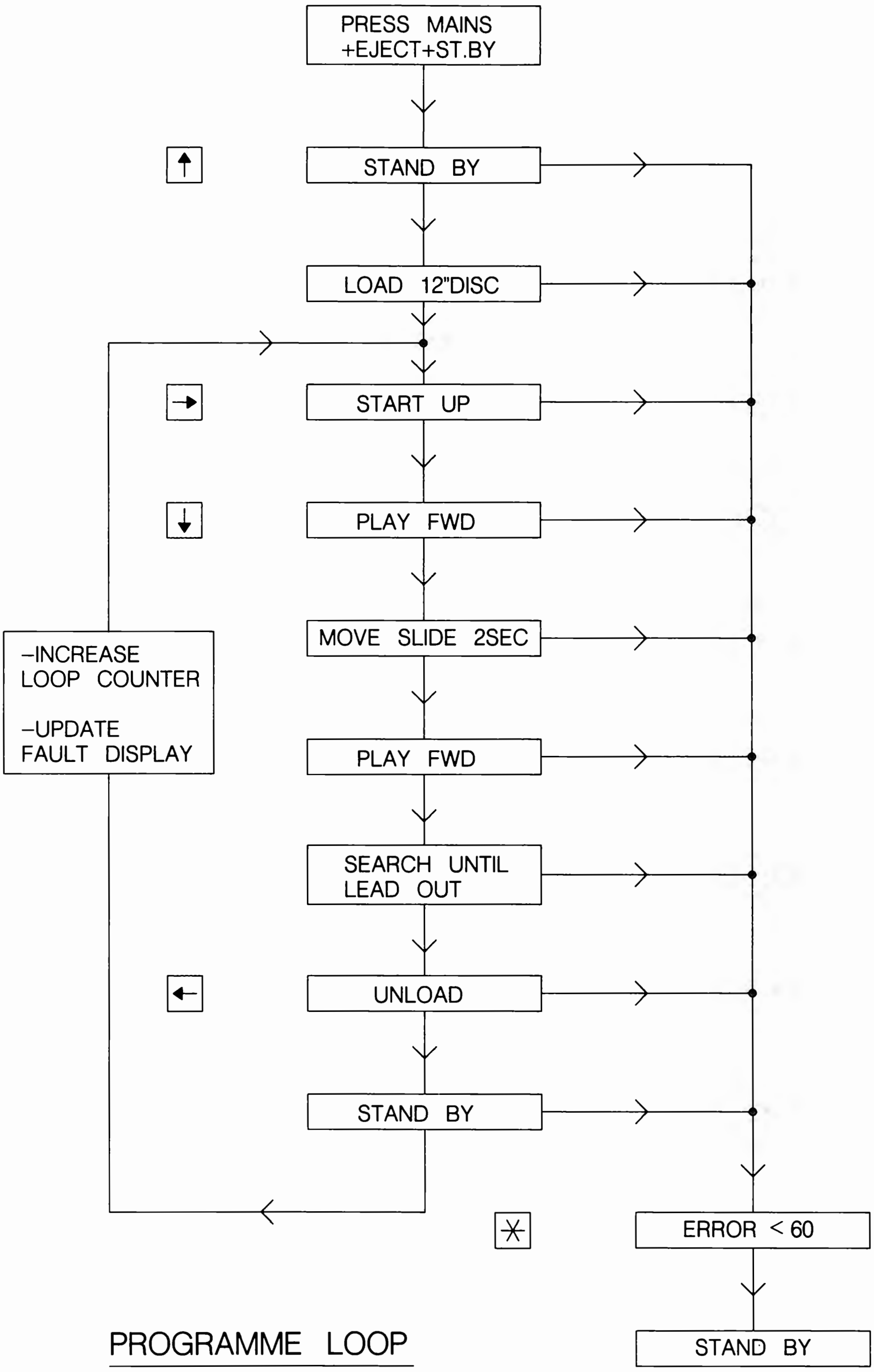
T27/716

d. *Programme loop in the self–test mode*

The following flow–chart shows what operations are carried out by the diagnostic software on behalf of the programme loop.



PROGRAMME LOOP

SELF–TEST MODE

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e. *Meaning of the error codes*

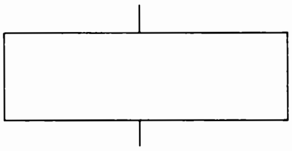
The survey below gives the meaning of the error codes shown on the picture screen. A detailed description of these error codes and a possible fault cause is assimilated in the subsequent repair method.

error code	description of error
1	tray is impeded in getting in or out
2	no disc reflection
3	SPI not found
4	time–out tilt
5	laser not on
6	not out of focus
7	not in focus after 5x (no rotation of disc)
8	motor speed error
9	framelock
10	motor slows down
11	laser not off
12	not out of focus after unloading
13	not switched into 'standby off' (time–out 2 sec.)
14	active 0–RPM without a LV disc at start up
15	laser out during MAIN 1
16	motor error during MAIN 1
17	no focus 20 steps after focus error
20	drive board inside LV player during hardware test
25	no REFV pulse at system start–up
26	REFV period > 64 msec
27	REFV pulse is not in conformity with NTSC/PAL standard
28	-
29	out of valid active video area, action:unload
30	no reference pulse
43	radial offset outside of window set to upper limit
44	radial offset outside of window set to lower limit
52	no 2ppr pulse
53	no lead–in code at start–up of player (diagnostics)
54	no active video area detected (diagnostics)
56	time–out (100 s) scan forward (diagnostics)
58	play forward error (diagnostics)
60	out of focus during 'main1'
61	out of focus at start–up (disc rotates)
62	detection of radial mirror movements fails during instant jump
63	goto time–out
64	no valid command
65	lead–in/lead–out
66	no valid 24–bit code
67	instant jump error in one of the previous jump(s)
68	time–out during track crossing instant jump
70	error 62 during 'scan'; corr. of slide with 1 fs.
71	radial mirror sensitivity > 900 µ/V
72	radial mirror sensitivity > 200 µ/V
73	a/d converted mirror pos. min. (out of field of view)
74	a/d converted mirror pos. max. (out of field of view)
75	SPI detected during master mode & slide moves inward. The slide is stopped by 'timer0'.
76	SPI protection is activated
79	apply for update of comm. pattern over zero steps
80	
81	no 24 bits
82	no 8 or F key
83	no valid 8 key code
84	no valid chapter code
85	lead–in code
86	lead–out code
87	time code
88	BCD error in picture no. X2X3
89	BCD error in picture no. X4X5
95	out of lock during main1 (only detec. for CAV discs)
96	no datic interrupt (no 24–bit code ?)
99	time–out during start–up 'diagnostics'
110	master mode: actual slide speed > limited speed
111	timer1 overflow / sw error
112	instant jump of > 51 tracks (limited to 51)
113	instant jump of 0 tracks
117	selection of 'slave mode' at high speed master mode
119	hwtest activated after detection of low level pin p3.5
120	hardware test is active
121	command sequence in undefined mode (diagnostics)
124	synchronisation error timing single track crossing
126	instant jump at high speed master mode (not executed)
127	instant jump during master mode (not executed)
133	error during 'step procedure'
137	re–initialisation of delay counter stand–by
151	re–init. delay counter stand–by
170	precontrol instant jump > 1step
171	precontrol error instant jump

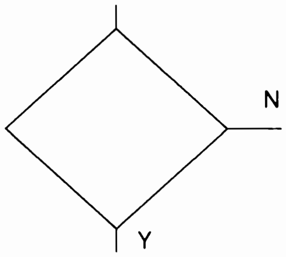
3. **Faultfinding**

a. *Meaning of the symbols used*

The symbols used in the test procedure and in the fault-finding tree have the following meaning:

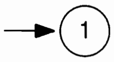


– action/operation to be carried out

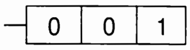


– decision

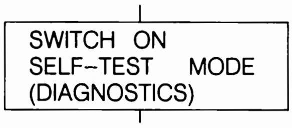
– Check module T or the circuits on this module



– Go on to block 1 in the faultfinding tree

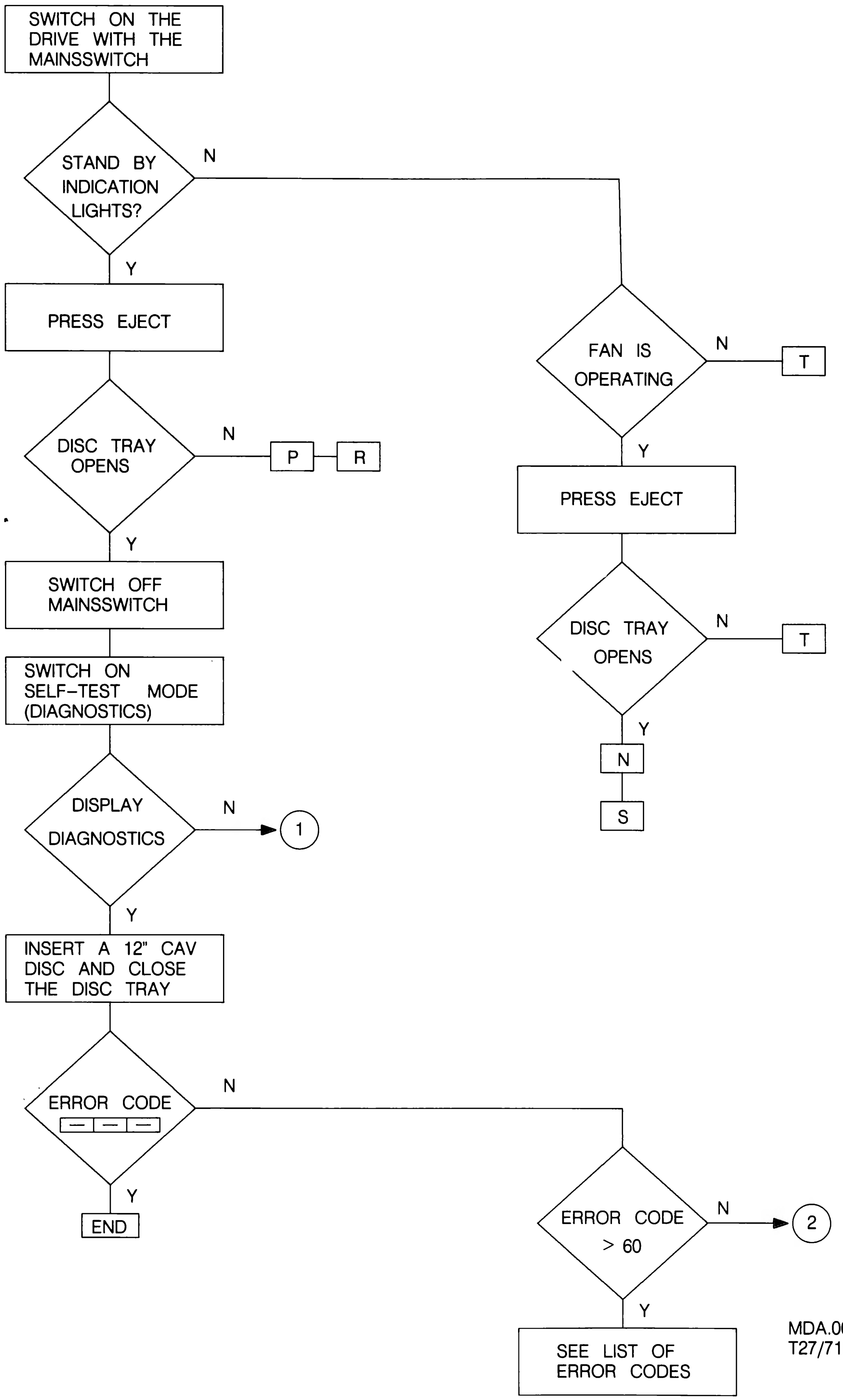


– Error code on the picture screen (no error = – – –)



– Switch on the drive by pressing STANDBY + EJECT and MAINS together.
Release buttons when display DIAGNOSTICS is visible

b. TEST PROCEDURE



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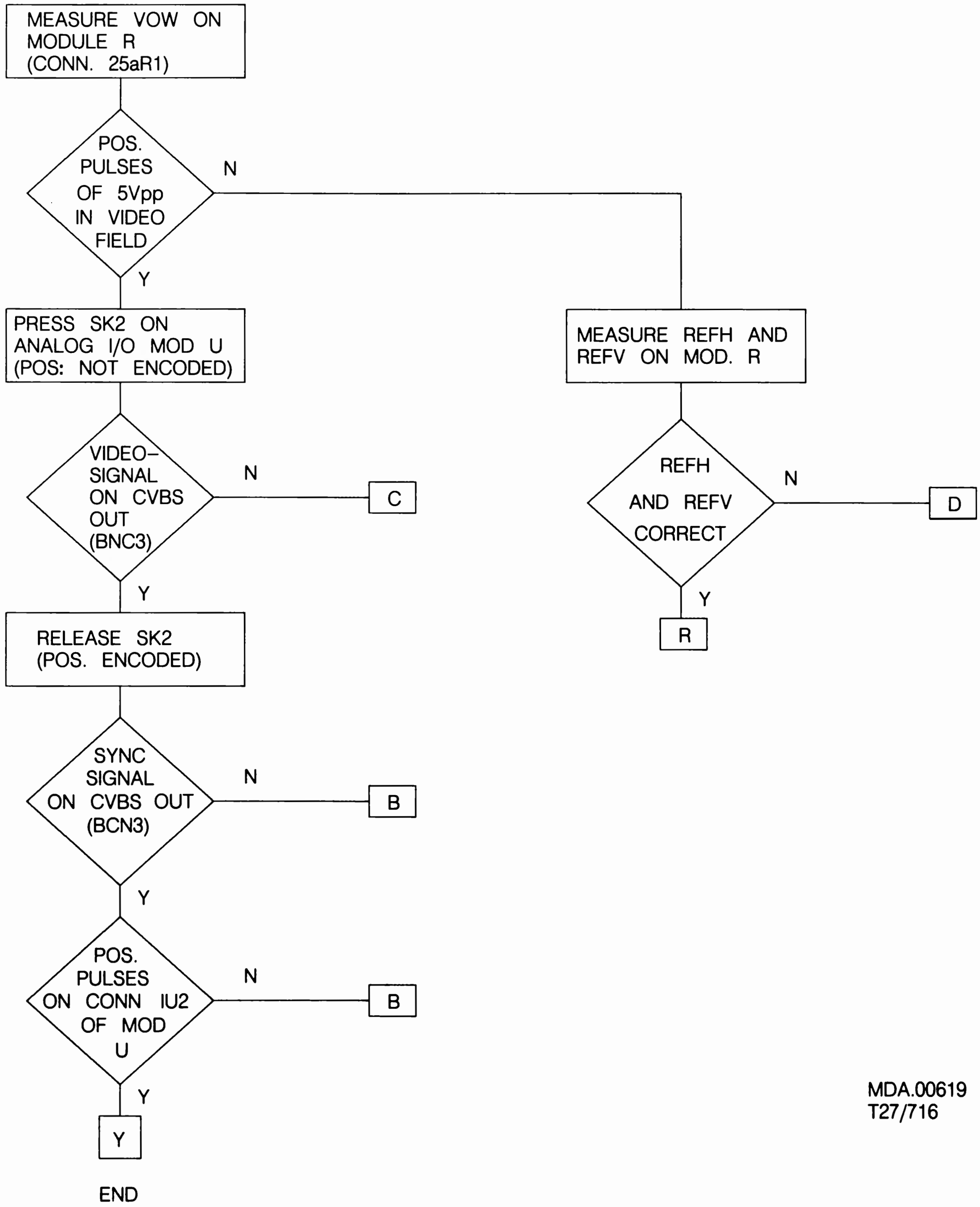
(1) NO DISPLAY



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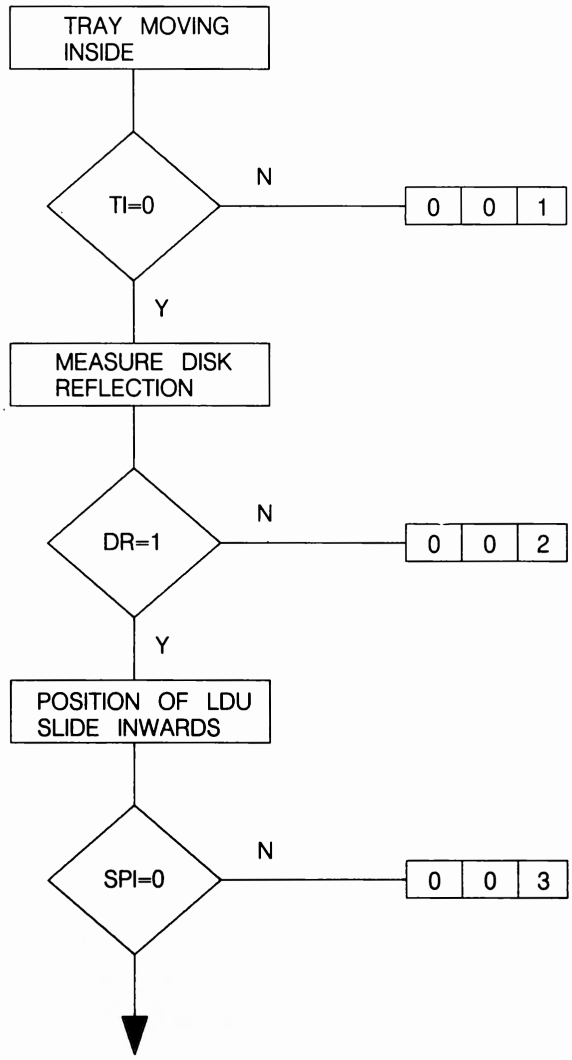
② ERROR CODE <60 (SELF TEST MODE)

AUTOMATIC GENERATED TEST LOOP;

A) START UP PROCEDURE



TRAY MEETS HINDRANCE

- CHECK THE MOVING OF THE DISC TRAY INWARDS THE DRIVE
- P R

NO DISC REFLECTION

- CHECK IF A DISK IS PRESENT IN THE TRAY
- CHECK ATC CIRCUIT IN OPTICAL DECK, MOD. Z

SPI NOT FOUND

- CHECK IF THE LDU SLIDE IS IN THE INWARD POSITION
- E R

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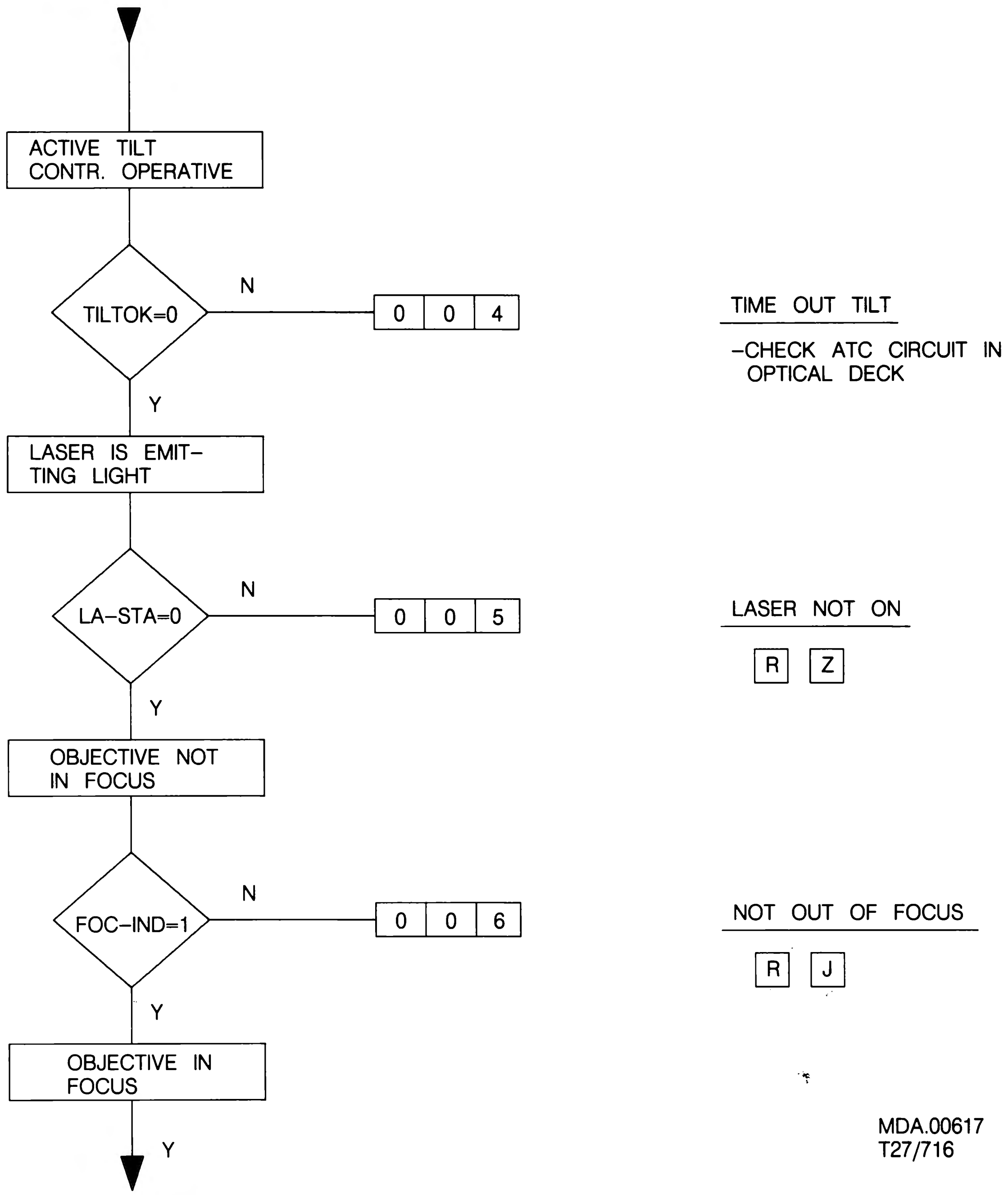

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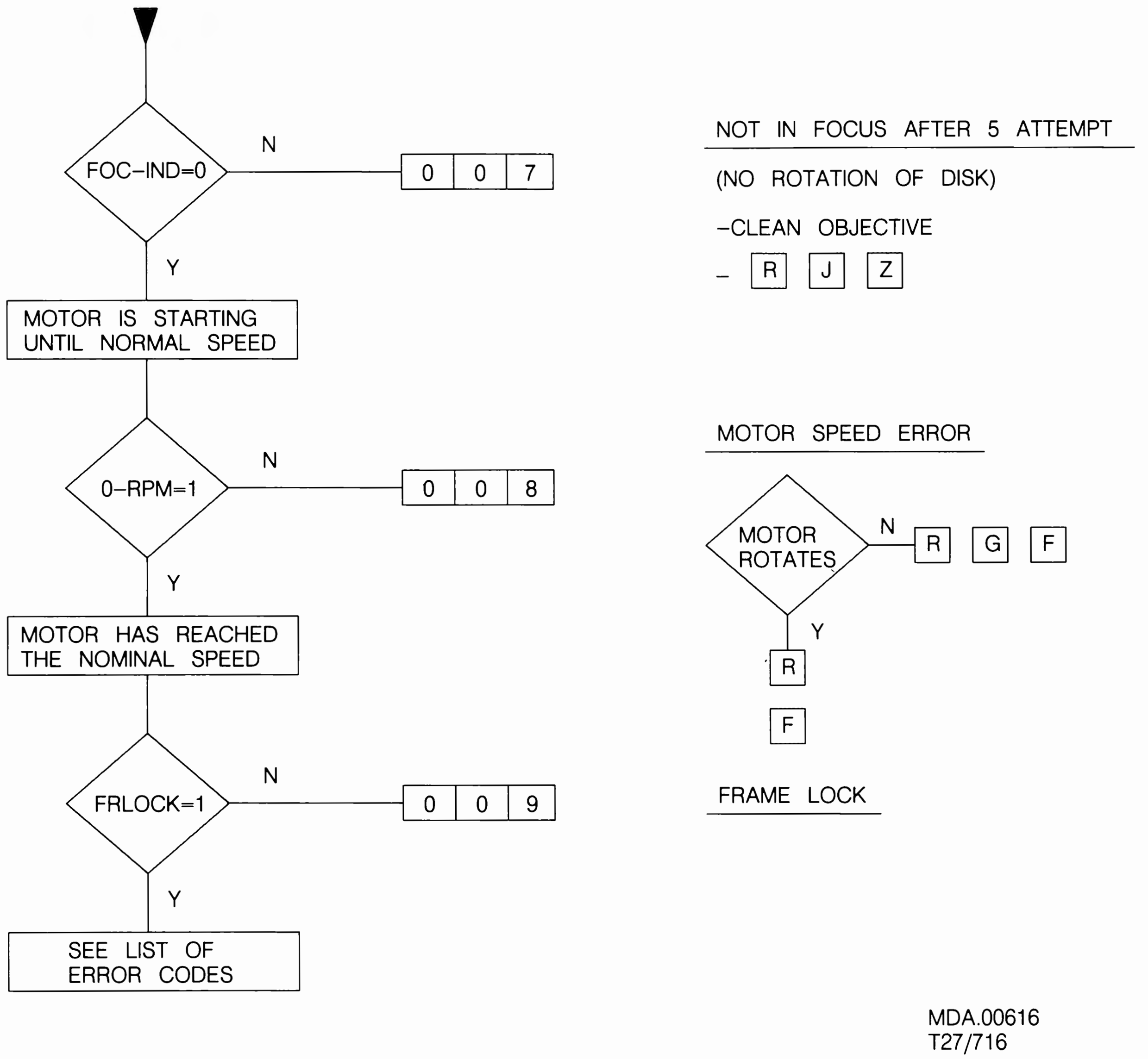

FOC–IND=0
N
0 0 7
Y
MOTOR IS STARTING UNTIL NORMAL SPEED
0–RPM=1
N
0 0 8
Y
MOTOR HAS REACHED THE NOMINAL SPEED
FRLOCK=1
N
0 0 9
Y
SEE LIST OF ERROR CODES
NOT IN FOCUS AFTER 5 ATTEMPT
(NO ROTATION OF DISK)
–CLEAN OBJECTIVE
– R J Z
MOTOR SPEED ERROR
MOTOR ROTATES
N
R G F
Y
R
F
FRAME LOCK
MDA.00616
T27/716

Circuit description

Chapter 7

Service
Service
Service

LaserVision

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Circuit Description

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Description des cicuits Schaltungsbeschreibung Kredsløbsbeskrivelse Kretsbeskrivelse Kretsbeskrivning Toimintaselostus Descrizione del circuito Description del circuito

Published by
Service Consumer Electronics

CS 7 874

CHAPTER 1 THE LASERVISION SYSTEM

Introduction

In the LaserVision system the video and audio information are stored on a disc in encoded form.
The information on the disc is scanned optically on a LaserVision disc drive and then converted into a CVBS signal as well as RGB signals suitable for a standard colour television receiver with Euroconnector. The information is stored on the disc along a spiral track in the form of pits; the disc is scanned from the centre to the outside. The length of the pits and their spacing are determined by the stored information.
The pits are 0.4 µm wide and approximately 0.1 µm deep. The track–to–track spacing is 1.6 to 1.8 µm (refer to Fig. 1). The overall length of the track on a 30 cm disc is about 34 kilometres!

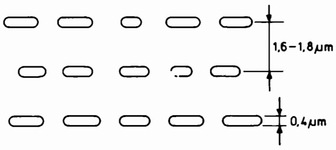

Fig. 1

The disc is made of a transparent plastic into which the pits are pressed. An extremely thin reflective layer of aluminium is added on top, followed by a protective coating that covers the whole. Two of these discs are glued together to form a double–sided disc. A cross section of the disc is shown in Fig. 2.

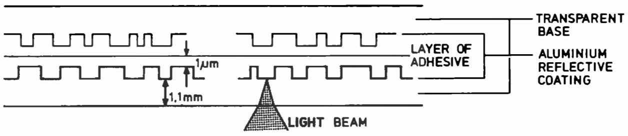

Fig. 2

A great advantage of the optical system is the contactless readout of the information on the disc, as a result of which wear of disc and read–out device is non–existant. A second advantage is the effective protection of the information on the disc against dust, fingerprints, etc. When taking a closer look at the beam path from the objective to the disc (refer to Fig. 3), we notice that at the place where the light cone enters the transparent base section the light cone's diameter is still fairly large.
Dust particles, etc. at this place exert very little influence; the light passes, as it were, around the dust particle. This highly effective protection of the information enables normal handling of the disc.

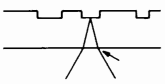

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Fig. 3

Optical read–out of the information on the disc takes place as follows:
The light beam from a ALGaAs semiconductor laser is focused on the disc by a lens (objective). In the absence of a pit practically the full amount of light is reflected. The reflected light passes through the objective and is then separated from the light beam going to the disc. The reflected light now falls on a photodiode; the amount of current that starts flowing through the diode is proportional to the amount of light falling on it.
When the light beam hits a pit, practically no light will be reflected due to the properties of the laser light and the depth of the pit; consequently, the current passing through the photodiode will be reduced.
In this way it is possible to convert the information on the disc into an electrical signal that is suitable for further processing to a standard videosignal in the disc drive.

Encoding of the signals on the disc

The videosignal is frequency modulated on a carrier (refer to Fig. 4a). Top sync level is situated at a frequency of 6.76 MHz, black level at a frequency of 7.1 MHz and white level at a frequency of 7.9 MHz. This results in a total frequency swing of 7.9 – 6.76 = 1.14 MHz.
Including this side bands the video FM signal encompasses a frequency range up to approximately 2.5 MHz at the lower side.
The two audio signals are equally frequency modulated on carriers of 683 kHz and 1066 kHz respectively. The frequency swing of the two channels is ± 100 kHz (refer to Fig. 4b).

Summing these three signals and next limiting them results in a pulse–width modulated signal (refer to Fig. 4c). The negative half periods of this signal determine the length of the pits, the positive half periods determine the spacing of the pits (refer to Fig. 4d).
Fig. 5 shows the entire frequency spectrum with associated recording levels of the video and audio RF signals.

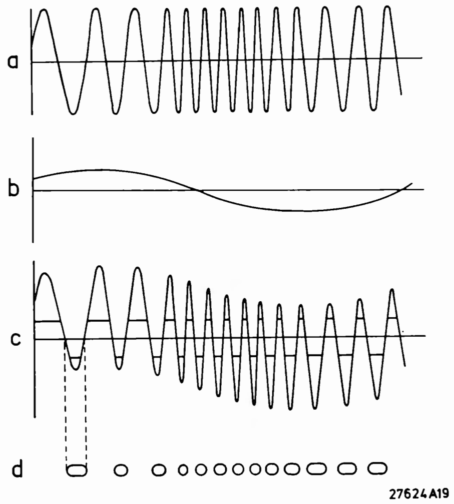

Fig. 4

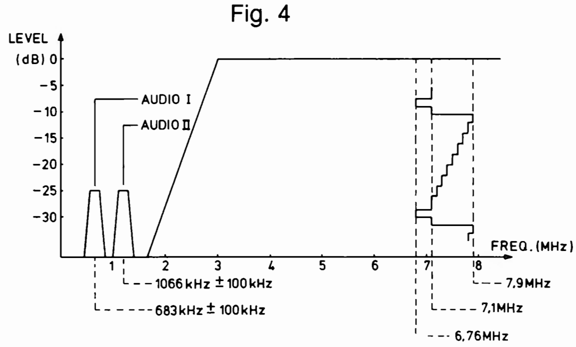

Fig. 5

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The encoded RF signals may be stored on the disc in two different ways:

1. The disc rotates at a constant speed (1500 rpm = 25 rps). At each revolution of the disc a complete TV picture is reproduced. This implies that the length of the track corresponding to one picture gradually increases from the centre of the disc to the outside. The frame sync pulses are situated on a diagonal. This type of disc is referred to as CAV disc (Constant Angular Velocity disc). Special playing modes like 'still picture', 'slow motion', 'fast forward' and 'reverse' are feasible with this type of disc only, since the frame sync pulses and, consequently, the frame blanking are situated on a diagonal. This allows jumping from one track to the next one or to the preceding one during the frame blanking period.
   The maximum playing time of a CAV disc is 36 minutes/side.

2. The track length of each frame on the disc is constant. This implies that the rotational speed of the disc decreases when scanning the disc from the inside to the outside, and that from 1500 rpm at the inside to 565 rpm at the outside of the disc. This type of disc is referred to as CLV disc (Constant Linear Velocity disc). No special playing modes can be realised with this type of disc, because the frame sync pulses and frame blanking are no longer on a diagonal, thus putting jumping from one track to the other out of the question.
   The maximum playing time of a CLV disc is 54 minutes per side. The disc drive is suited for both types of discs.

In addition to the video and audio information, the disc contains a number of special codes, inserted in the frame blanking periods.
Test signals have been inserted during the lines 19, 20, 332, 333. Digital codes for various purposes have been inserted during the lines 16, 17, 18, 329, 330, 331.
These signals have the following functions:

Lead–in tracks

A minimum of 900 tracks prior to the start of the actual programme contain a start code which sends the read–out objective to the beginning of the programme at nine times the normal speed.

Lead–out tracks

A minimum of 600 tracks immediately after the end of the programme contain an end code which sends the read–out objective back to the beginning at 75 times normal speed. Video and audio signals are muted during the return period.

Programme area

Here a distinction has to be made between CAV and CLV types of discs.

CAV discs

1. Picture code consisting of a picture number by means of which each individual picture of a programme can be identified.
   The number may be displayed on the monitor screen,if desired.
   The picture number code is always present in the first field of each complete television frame. The second field may contain a stop code to switch the disc drive to STILL PICTURE mode.
2. Chapter code consisting of a chapter number by means of which a search action can be automatically stopped as soon as the start of the relevant chapter is reached. The chapter number may also be displayed on the monitor screen, if desired.
   The presence of stop code and chapter code is optional and depends on the programme content.

CLV discs

1. A normal play code is always present in CLV discs. This code disables the special modes of operation of the disc drive.
2. Instead of a picture number code a time code is present in LV discs. It contains a time coding with hour and minutes indication showing the time elapsed since the start of the programme. This time may be displayed on the monitor screen,if desired.

Focusing

The objective used to read the information on the disc has a very small depth of focus, that is, maximum 1.5 μm. In view of tolerances in disc and in disc drive construction this accuracy can only be realised by means of a servo-–control system that continuously verifies and corrects the focusing of the objective. For this purpose the objective is mounted in a magnet so as to allow vertical motion. Around the objective and firmly attached to it, a coil has been mounted. By feeding a current through the coil, the objective will move more or less upwards, depending on the current intensity. Fig. 6 shows a cross–sectional view of the objective plus coil and magnet.
The system is very much similar to a loudspeaker system.

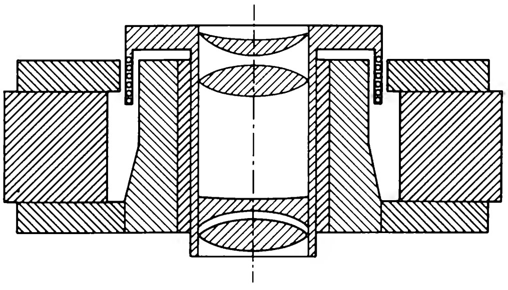

Fig. 6

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The objective is driven in the following way:
The light reflected by the disc is focused on the photodiodes by the objective. On its way to the diodes the reflected beam passes an astigmatic lens system, like a cylinder lens.
Unlike a spherical lens, an astigmatic lens does not have one single focal point, but two focal lines at some distance from each other and at right angles to each other. Between the focal lines a plane exists where a circular picture is formed. When the disc is out of focus with respect to the objective, that is too far from or too close to the objective, the astigmatism will modify the shape of the picture from the focused state (circular picture) to an elliptical picture. The direction of the ellipsis' axes is determined by the fact whether the disc is too far from or too close to the objective. The photodiode that converts the light variations into an RF signal is composed of four quadrants A, B, C and D (refer to Fig. 7). When the objective is in focus, all four quadrants receive equal amounts of light.
When the objective is out of focus, either A and B or C and D receive more light. The quadrants are interconnected crosswise. The sum of the signals over A, B, C and D receive more light. The quadrants are interconnected crosswise. The sum of the signals over A, B, C and D constitutes the RF signal. The difference signal (A+B) – (C+D) is the drive signal for the objective.

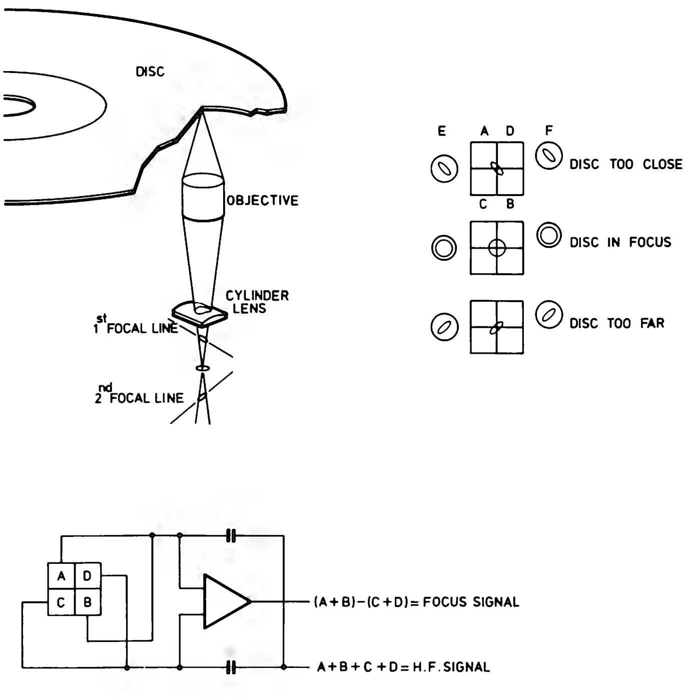

Fig. 7

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Radial tracking

The information on the disc is contained in a spiral track that is read from the inside to the outside. This implies that objective – in order to be capable of following the track – has also to move from the centre of the disc to the outside. For this purpose the objective and all associated components which constitute the optical system are mounted on a slide, driven by a motor and moving radially under the disc.
The light has to follow the track on the disc with an accuracy of approximately 0.1 µm.
Tolerances in player and disc may cause a track wobble of 130 µm. It will be clear that the slide is incapable of following this wobble at a rotational speed of 25 rps.

To obtain the required accuracy a movable mirror has been inserted in the light path under the objective; this mirror allows to move the light spot radially over the disc.

A magnet is attached to the mirror. Around the mirror a coil is mounted. When a current flows through the coil, the intensity and the direction of this current determine to what extent the mirror will pivot to the left or to the right (refer to Fig. 8).
Driving of the mirror is obtained as follows:
In the optical system, apart from the main beam for track scanning, two further auxiliary light beams are formed whose impact is slightly displaced with respect to the track's centre line, in opposite directions.
The light spots formed on the disc by the two auxiliary light beams fall partly on the track and partly outside the left or right edge of the track. The objective focuses these light spots on two separate photodiodes situated at either side of the signal diodes (E and F in Fig. 7). When the track is followed correctly, the signals coming from each diode will be equal. When tracking is less optimal, it depends on the direction of deviation which diode output will exceed that of the other diode (Refer to Fig. 9).
The difference between both signals is – after amplification – used to drive the mirror. When the average voltage across the mirror coil is positive or negative, the slide motor will be controlled until the average voltage is again 0 (zero).

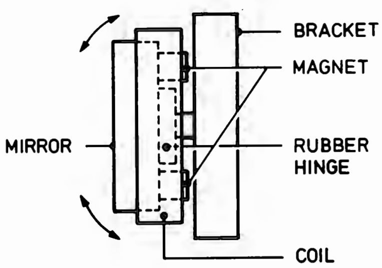

Fig. 8 27628A19A

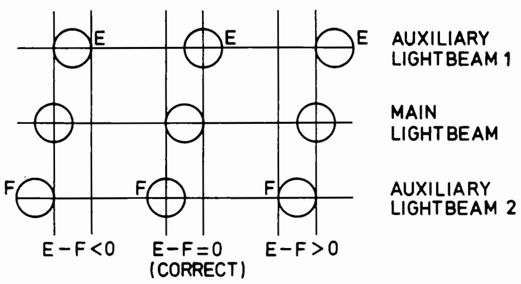

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Fig. 9

TIME BASE CORRECTION

As known, a TV picture consists of lines that are written in an accurately laid down time (64 µsec for the PAL system). Deviations from this time cause a distorted picture and phase errors in the colour signal which may lead to dropping out of the colour.
The video signal of the disc drive should also meet this requirement of constancy of the time base to be able to give an undistorted picture with colour.
The presence of several tolerances (disc, centring, motor) results in variations in the line time of the video signal.

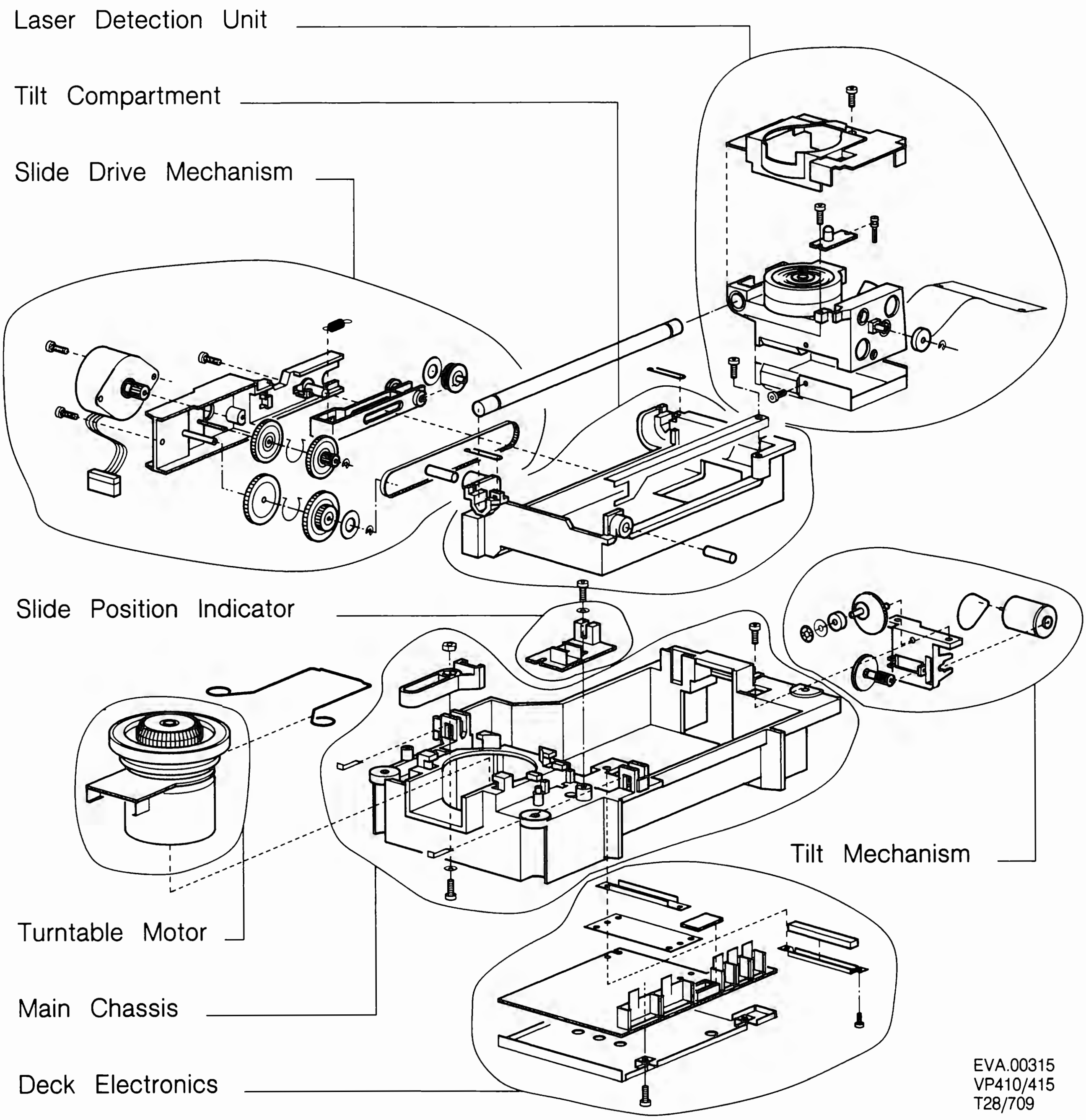
Now the maximum permissible deviation from the time base to give a stable picture with every TV receiver is 5 nsec. To reach this value it will first of all be necessary to keep the speed of the turntable motor as constant as possible. To achieve this the phase of the line sync pulses is compared with the phase of pulses with the line frequency coming from a crystal oscillator. The resultant control voltage is used to drive the turntable motor. It is clear, however, that variations in speed with a frequency of 25 Hz and higher cannot be corrected by this control.
For the correction of these errors use is made of a CCD (charge coupled device) which functions as a variable delay line for the great time errors (+/− 17µsec) and a variable LC delay line for fine control (+/− 50 nsec).

The CCD is driven by a signal which is obtained through comparison of the phase of crystal–controlled reference signal with the line frequency and line frequency pulses of the disc video signal.
Since the line sync pulses themselves are not suited for an accurate enough measurement of the time difference use is made of a signal having a frequency of 3.75 MHz (240x the line frequency) which has been laid down on the disc at the level of the peak sync pulses.
If the same zero crossing of the 3.75 MHz signal is used for every line sync pulse, the actual line time can be measured sufficiently accurately. The time base correction makes it possible to connect the disc drive to any TV set.

GENLOCK

Genlock serves to synchronize the video signal of the disc drive with the video signal of another source. I.e. the line and frame pulses of both signals are in phase (sync lock). This is necessary to enable interference–free switching–over of both video signals. Locking is done by controlling the revolution speed of the disc and hence the phase of the line and frame pulses.

Fig.OD1 OPTICAL DECK



THE OPTICAL DECK

The optical deck reads the information from the video disc by means of a laser beam. The modulated laser light is transferred into an electrical signal which is further processed in the electronics of the player.

The deck consists of a main chassis, containing the following parts (see Fig. OD1):

- The Laser detection Unit (LDU) to read the information from the video disc.
- The slide drive mechanism to move the LDU under the disc.
- The turntable motor to spin the disc.
- The tilt compartment which causes an angular (and vertical) move of the LDU under the disc.
- The tilt mechanism to drive the tilt compartment.
- The slide position indicator to indicate the starting position of the slide.
- The deck electronics where the signals from the LDU and tilt control are processed.

The Laser Detection Unit (LDU)

The LDU reads the information from the video disc and delivers electrical signals to be processed further. The principle of the unit has been drawn in Fig. OD2.

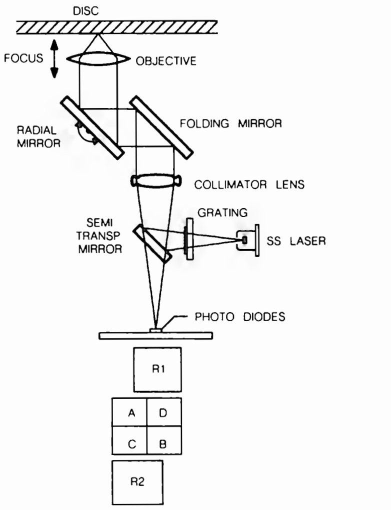


Fig OD2 LIGHT PATH

A Solid State laser emits a diverging laser beam. The power of the beam is 3mW and the emitted light has a wavelength of 780 nm. The laser is of the Aluminium Gallium Arsenide (AlGaAs) type.
Just in front of the laser, a grating plate has been situated, causing the laser beam to be split into a main beam and two auxiliary beams, to be used for radial tracking.
After the grating, the beam reflects partly on the surface of a semi transparent mirror. The reflected beam, still diverging, passes through a collimator lens causing the beam to proceed exactly parallel. A folding mirror projects the beam onto a radial mirror which is activated by the radial correction signal.
Eventually the objective focusses the beam on the surface of the video disc. The objective is driven in vertical direction by the focus correction signal.
The laser light that is reflected by the video disc, containing the disc-information, returns by the same path as described before, so via the objective, radial and folding mirror, through the collimator lens to the semi transparent mirror.

On this mirror, the laser light is partly reflected back into the laser, but enough light is going through the mirror to be detected on the photodiodes. These diodes consist of a quadrant diode and 2 auxiliary diodes R1 and R2.
The quadrant diode delivers the signals AB CD to compose the HF– and focus signal, diodes R1 and R2 deliver the radial tracking signals.
Fig. OD3 shows the detailed construction of the LDU.

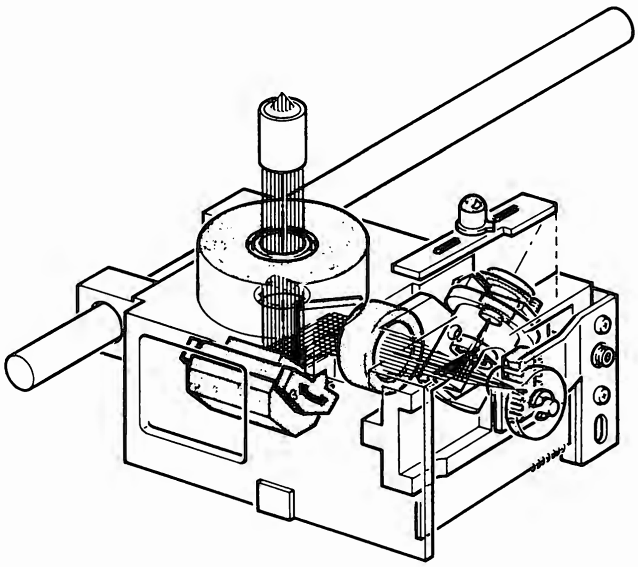


FIG. OD3 LASER DETECTION UNIT 42 043 A12

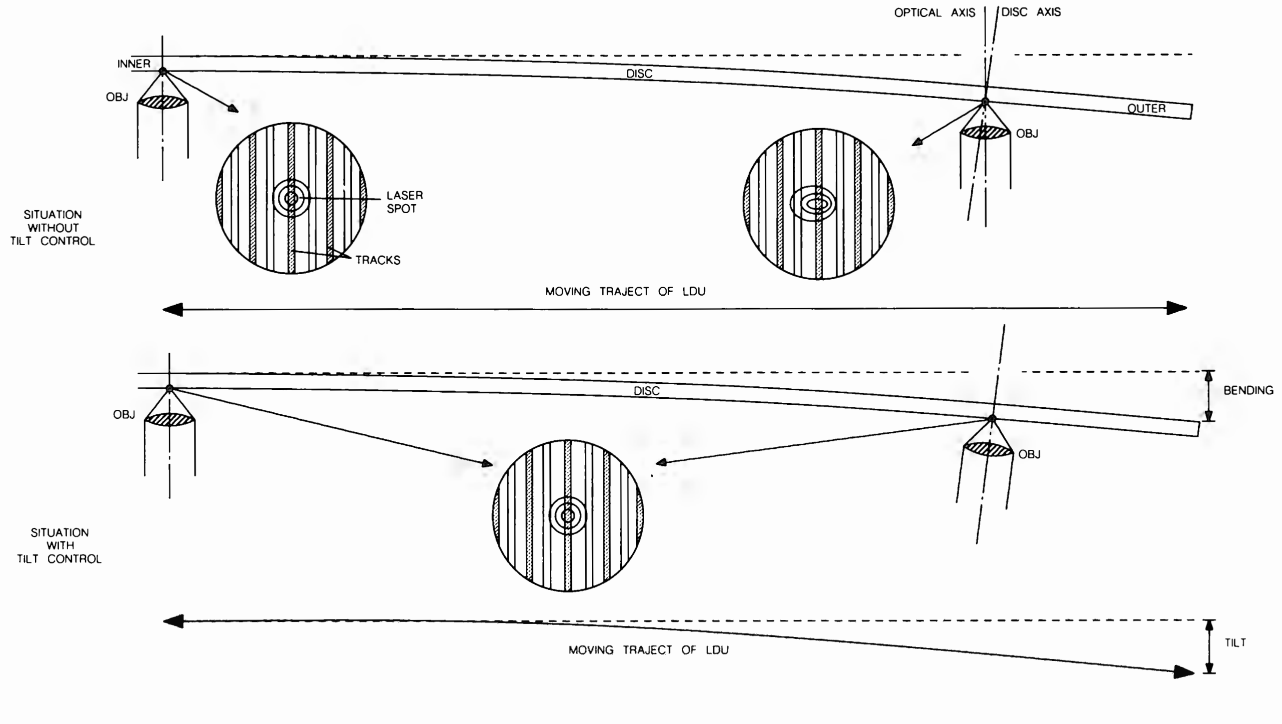


Fig OD4 ACTIVE TILT CONTROL PRINCIPLE

Active Tilt Control (ATC)

- Principle (see Fig. OD4)
When a video disc is put on the turntable it will bend, caused by its own weight (umbrella shaped).

The LDU which is moving in a horizontal plane under the disc will have a different distance related to the surface of the disc when reading in the beginning of the disc or at the outer side of the disc. At the outer side, the optical axis of the LDU is not perpendicular to the disc surface anymore. In this area, the focussed laser spot is distorted, causing optical cross–talk between the tracks. Active Tilt Control means that the LDU is moved in angular direction to achieve that the LDU is always perpendicular to the disc surface, so that the cross–talk is minimal. Therefore the distance between LDU and disc has to be measured to detect a possible deviation.

- Measuring the distance
To measure the distance between the LDU and the disc surface, a LED is mounted on the LDU which emits infrared light.

The light that is reflected on the disc surface, hits receiving diodes D1 and D2 (see Fig. OD5). When the reflected light on D1 equals D2, the position of the LED (and of the LDU) related to the disc, is correct. If D1 differs from D2, a positive or negative error signal will be generated, which drives a DC motor. This so–called tilt motor corrects the position of the LDU, until D1 equals D2.

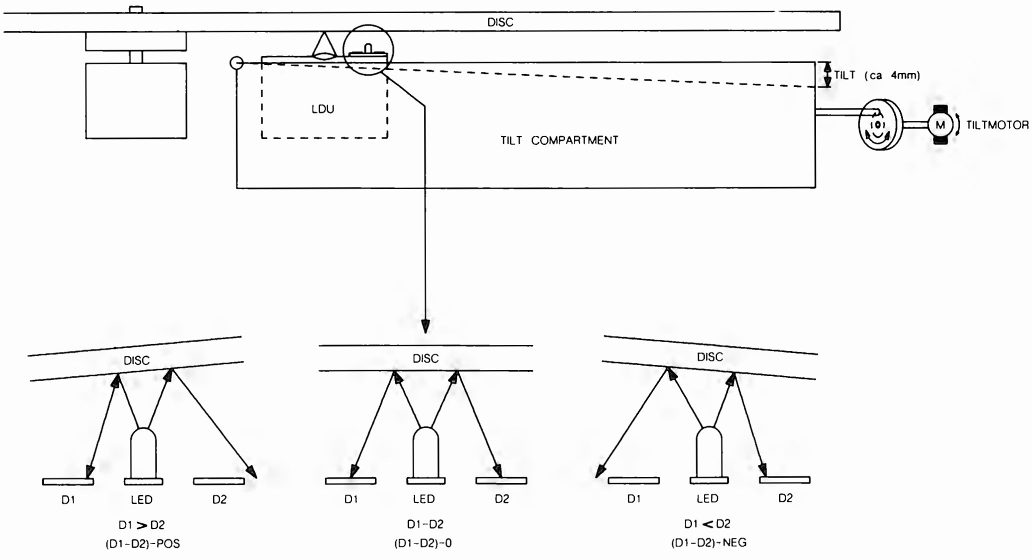


Fig.OD5 ACTIVE TILT CONTROL

CHAPTER 2 VP400 series

Introduction

The VP400 series is a new generation of LaserVision disc drives with all the versatile LaserVision facilities, such as picture or chapter search, moving pictures, still frames, forward, reverse and variable speed. These facilities can be programmed through a separate computer for interactive applications.

characteristic of these disc drives:
- Front loading
- Solid–state laser
- Computer control via RS232C interface.
- RGB output for full–bandwidth moving or still pictures.
- Functional modular design.
- Average random access time ⩽ 1 sec.
- Instant jump of up to 50 frames in either direction.
- Electronic timebase correction.
- Genlock external video synchronisation.
- Infra–red/wired or SCART RC–5 remote control.
- Programmable with the remote control handset.
- Auto replay via replay switch.

Depending on the specific type of the VP400 generation, more features are created.

Audio/video signal path

The audio and video information on the video disc has been fixed in the form of pits.The information can be read by means of a laser beam having a wavelength of 780nm. The laser light modulated by the disc falls on the photodiode present and is thus converted into an electrical signal. This signal is a highfrequency signal which is amplified on module Z, see the block diagram of the audio/video signal path. The output signal of this module, HF–OUT 1, goes to module K where it is in the first instance split into an h.f. audio and an h.f. video signal. The h.f. audio signal goes as HF–AUD to module H on behalf of timebase correction. The h.f. video signal is also demodulated on module K and gets amplification correction by means of the MTF signal. The demodulated composite video signal, CV–DEM, goes to module L where drop–out correction takes place.

Drop–out correction is realized on module L by filling it in on a video line which contains a drop–out, together with the video contents of the preceding video line. To achieve this the video signal is delayed one line time (64µs) and, if a drop–out is detected, filled in in the passing video signal. This is possible because a switch, operated by the drop–out detector, can select the "direct" video or the delayed video. On this module the MTF signal is created too. This is done by measuring the amplitude of the colour burst signal in the video signal and realizing a dc voltage dependent on this value (the MTF signal). The output signal of module L is fed to module H to obtain timebase correction just like the h.f. signal.

On module H the h.f. signal (HF–AUD) and the compositie video signal (CV–DOC) are both led through a CCD memory IC and as a result the signals get a delay which depends on the clock frequency offered. The clock frequency is determined by the VCO present which is controlled by the TANG–ER signal (tangential or timebase error signal). The correction which takes place by the TANG–ER signal is the coarse correction. Next the audio and video signal is led through a variable LC delay line with a delay that depends on the BURST–ER signal. This BURST–ER signal is the result of a phase comparison of the disc video signal (CV–TBM) with a reference signal derived from the reference source on module D. The timebase correction by means of the BURST–ER signal is a fine adjustment. The timebase corrected h.f. audio signal (HFATBC) and composite video signal (CV–TBC) are processed further on modules A and C resp.

On module A the HFATBC is split into two paths on behalf of demodulation of the two audio channels. On this module drop–out detection takes place too where, in the case of a drop–out, the l.f. audio signal is kept at the last level just before the dropout (track and hold principle). The two output signals (AUD1 and AUD2) go to analog I/O module U.

The two low–frequency signals AUD1 and AUD2 enter at the analog I/O module U where selection takes place between the externally offered audio signals (EXT AUD1 and EXT AUD2) and the internal audio signals. The audio signals can also be switched off by means of switching signals AUD1ON and AUD2ON. A beep can be added to the audio signals dependent on the A–SYNT command of the drive processor (module R). The two audio signals are available on 2 BNC connectors at the rear of the disc drive and also on the Euroconnector.

The composite video signal (CV–TBC) goes from module H to module C where it is processed further. First of all there is selection possible between the internal video and composite sync (CS–REF) of reference source module D. This among other things in connection with sync during mute. Next switching is possible between the internal video or reference sync and the externally offered composite video signal (CV–EXT), coming from analog I/O module U.
The signal further receives a required black level clamping and, if desired, the index insert. For this purpose there are two signals $\overline{\text{VOBN}}$ to see to an index background and VOW for the insert of the index information lying at white level. From the video signal the line frequency sandcastle signal (SC) is generated by means of a sync separator and with the VBL (vertical blanking) signal this signal also receives the frame frequency component. The video signal is buffered along two paths, with one CVBS signal going to module B and the other CVBS signal being stripped of the special burst signal, which is a standard presence in the video signal. The latter signal goes to analog I/O module U.

The dc level of the CVBS2 signal which arrives at module U is restored and goes as TXT CVBS to the TXT section of this module. Moreover, a possible selection takes place between the externally connected video signal (CVBS IN) and the TXT CVBS signal. Selection can be done by means of switching signal CV–E/$\overline{\text{I}}$. The output signal of this switch goes to manual switch SK2 and is as CVBS OUT available on a BNC connector at the rear of the disc drive. With switch SK2 a selection can take place between "not encoded" video and "encoded" video. The internal composite signal CVBS2 is transferred directly from the disc but is as such not suited for connection to monitors when use is made of the special playing possibilities of the disc drive. The encoded CVBS is suited for monitor use but has a limited bandwidth (3 MHz).

The CVBS signal of module C (with special burst) is on module B decoded into RGB with complete bandwidth. For this purpose the CVBS signal is split into a luminance and a chrominance part. The chroma signal is decoded into the colour difference signals R–Y and B–Y. Together with the luminance signal LUM encoding into CVBS takes place on module U. Colour signals R, G and B come from the RGB matrix on module B and go, via module U, to the video mixer module Y in the sandwich section of VP415.

Whether or not on module Y mixed with the RGB signals of a computer to be connected externally, where the mode of mixing depends on signals VP0, VP1 and VP2 the outgoing RGB signals go to the Euroconnector via module U. Thus the RGB signals are with complete bandwidth (5 MHz) available for a monitor to be connected, just like the encoded CVBS signal (bandwidth 3 MHz).

Fig. SP 1 AUDIO/VIDEO SIGNAL PATH

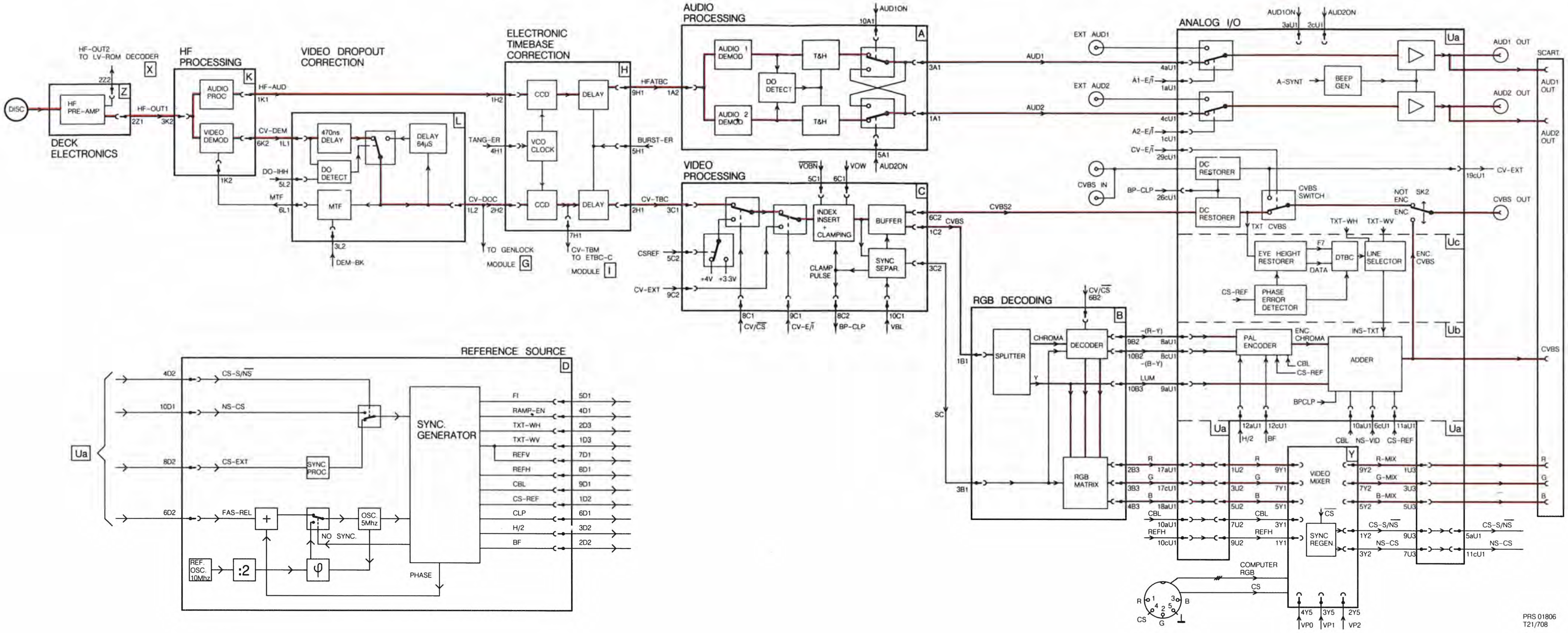


Fig. CR 1 BLOCKDIAGRAM CONTROL ROUTES

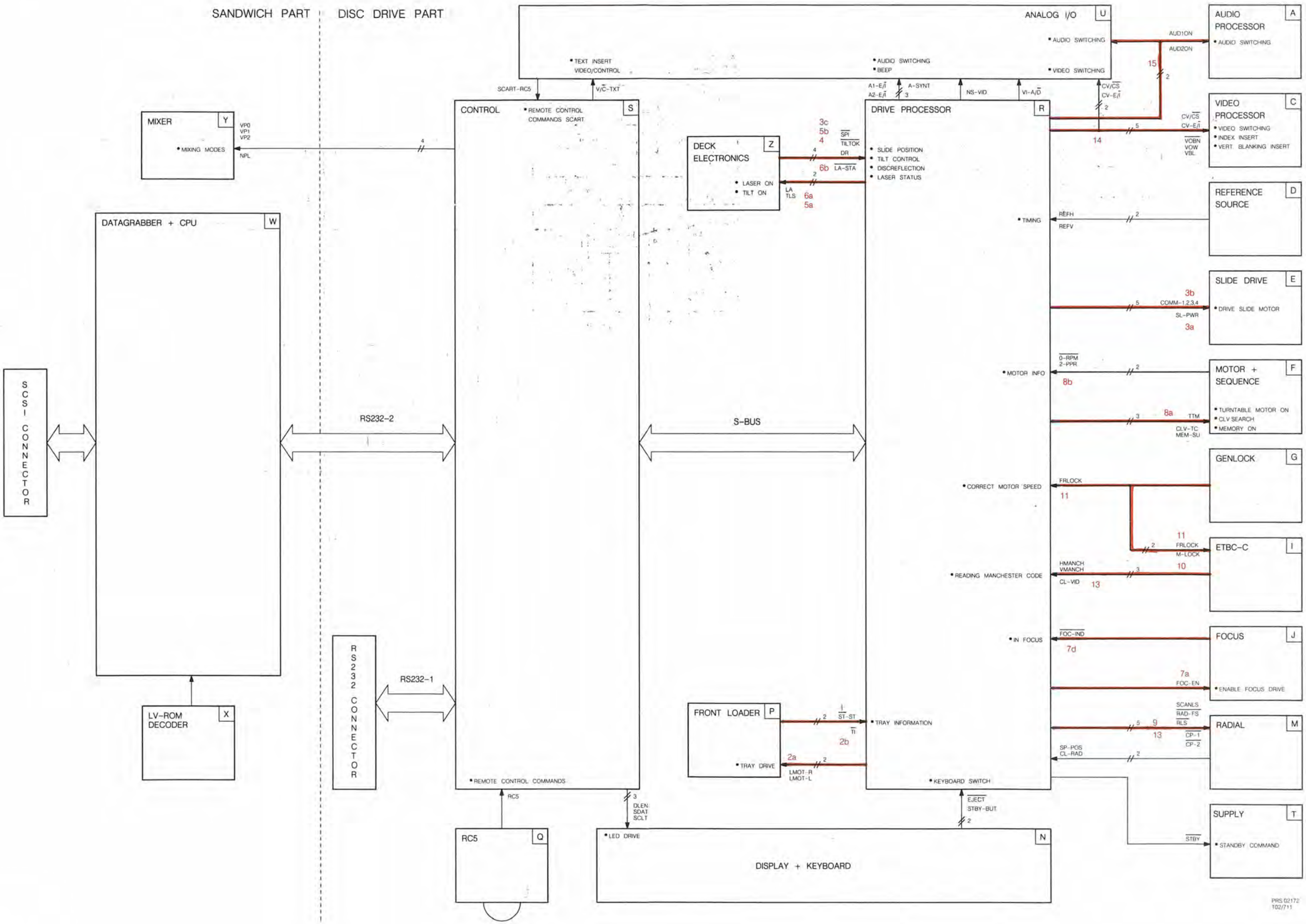
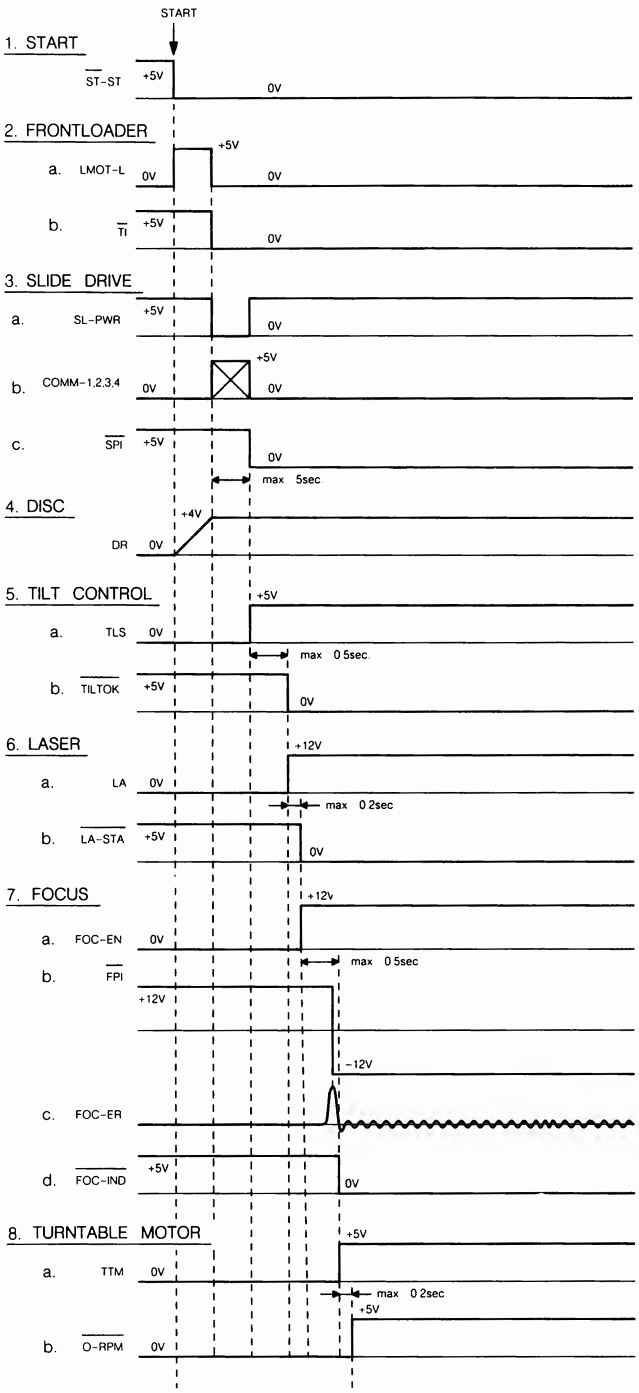


Fig. CR2 START–UP SEQUENCE



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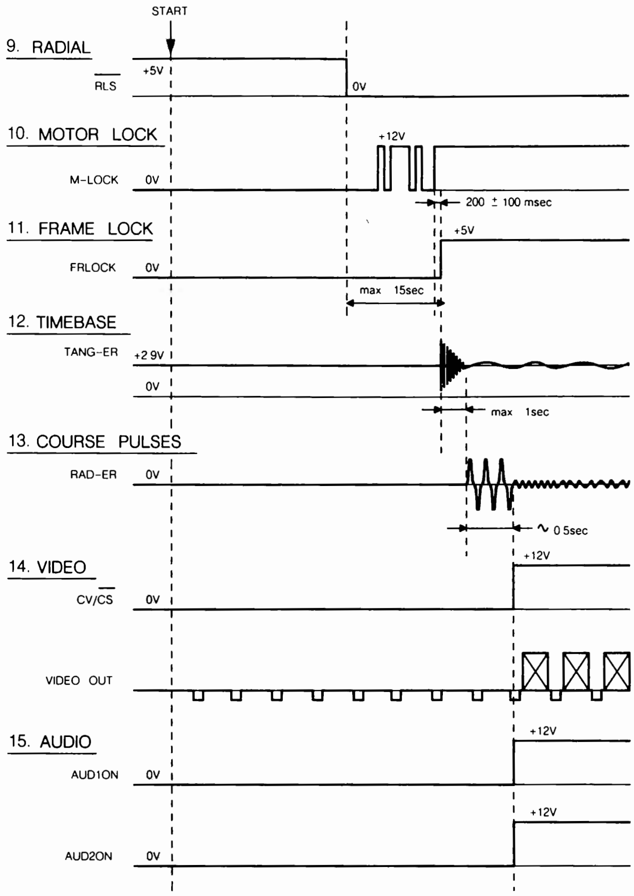

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Control Routes

The control and drive section of the VP415 disc drive is determined by two modules, viz CONTROL PROCESSOR MODULE S and DRIVE PROCESSOR MODULE R. These modules determine the actions of the disc drive which is composed of a number of functional modules. See the block diagram of the control routes in Fig. CR1. The control processor and the drive processor communicate via the S–bus.

– The **control processor** has interactions with the outer world; via a communication similar to the RS232 bus (RS232–2 bus) with the sandwich part of the disc drive, CPU and data grabber module W and thus via the SCSI connector with a computer to be connected externally. Moreover, the RS232 connector (RS232–1 bus) is directly connected to module S. The control processor controls the remote control communication (RC5); namely the infrared or wired RC5 commands, and the SCART–RC5 commands. Via lines DLEN, SDAT and SCLT the control processor drives the LEDS on display + keyboard module N. On behalf of the different video mixing possibilities which are realized on video mixer module Y in the sandwich section, the control processor gives signals VP0, VP1 and VP2. The NPL signal is not used.

– The **drive processor** has various main tasks:

a) To accept and interpret commands from control module S
b) Radial tracking and access
c) Manchester code reading
d) Display on screen drive
e) Start–up sequence of the disc drive
f) Local control: 'stand–by' and 'eject'.
g) Audio and video switching
h) Service diagnostics

sub a) Command inputs from and responses to module S go via the S–bus. Please refer to the S–bus section for detailed information on the operation of the S–bus.

sub b) During start–up the voltage on the radial mirror is studied. By means of the actual mirror position the slide is displaced, if necessary, under certain conditions. The required signals of radial module M are SP–POS and CL–RAD.

sub c) The manchester code is present in the video read from the disc and gives information on picture numbers, chapter code, stop code and CLV code. This information is necessary for the drive processor i.a. to give the index contents, search actions and instant jump. The required signals of ETBC–C module I are VMANCH, HMANCH and CL–VID.

sub d) To give index information on a connected picture screen a character generator is present on the drive processor. Synchronized to the video signal present an index background signal (VOBN) and an index information signal (VOW) are inserted in the video on module C.

sub e) **Start–up sequence**. The drive processor takes care of and checks the start–up procedure. After the disc has been inserted on the tray and the tray has been pushed in the start–up procedure is actuated, provided the disc drive is in stand–by. The start–up sequence has been elaborated in timing diagrams, to be seen in Fig. CR2. The numbered steps in this sequence can be found back in the block diagram of the control routes in Fig. CR1. In this way one can see in which sequence the various modules are energized by drive processor module R. In the story below the required signals have been named followed by the number corresponding with the timing diagrams.
After the start, the pushing in of the tray with 'start–stop' (ST–ST: 1) as command, we see the following:

* The pulling in of the front loader (LMOT–L: 2a) with as control the "tray inside" (TI: 2b) signal.
* Bringing the slide to the initial position (SL–PWR: 3a and COMM–1,2,3,4: 3b) with as control the 'slide position indication' (SPI: 3c) signal.
* Detection of the presence of a disc by means of a photosensor and control signal 'disc reflection' (DR: 4).
* Activation of the tilt control (TLS: 5a) with as control the 'tilt ok" (TILTOK: 5b) signal.
* Switching on of the laser (LA: 6a) with as control the 'laser status' (LA–STA: 6b) signal.
* Activation of the focus control by means of the 'focus enable' (FOC–EN: 7a) signal. If focus is found, the deck electronics, module Z, give the 'focus position indication' (FPI: 7b) signal to focus module J. This FPI signal gives together with the zero crossing of the 'focus error' (FO-C–ER: 7c) signal, , the control command for the drive processor, namely the 'focus indication' (FOC–IND: 7d) signal.
* The turntable motor is brought to the correct speed after the 'turntable motor' (TTM: 8a) command. The control is the '0 rpm' (0–RPM: 8b) signal.
* The loop for the radial tracking is closed with the "radial loop switch' (RLS: 9) signal.
* The motor is locked to the read–out video of the disc with as indication to timebase correction module I, the 'motor lock' (M–LOCK: 10) signal.
* The synchronization of the video signal of the disc is then locked to the reference source on module D with as control to the drive processor the 'frame lock' (FRLOCK: 11) signal.
* The control of the timebase correction becomes active, resulting in a correcting signal, namely the 'tangential error' (TANGER: 12) signal. This signal goes from module I to ETBC–B module H.
* The lead–in code is read by the drive processor by means of the HMANCH, VMANCH and CL–VID signals. The drive processor will give course pulses for the radial mirror up to picture 1 to radial module M, which results in the 'radial error' signal as indicated (RAD–ER: 13).
* During start–up a sync signal is present on each video and sync output, derived from reference source module D. With the 'composite video / composite sync' (CV/CS: 14) command the video read from the disc is put on the outputs. On a connected monitor a locked picture with colour will appear.
* The audio lines switch over, because of the 'audio 1 on' and 'audio 2 on' (AUD1ON, AUD2ON: 15) signals. The audio LEDs will light up just like the CAV or CLV LED, dependent on the disc.

sub f) On the front of the disc drive you will find two keys, 'eject' and 'stand–by', which pass the related commands directly to the drive processor via display + keyboard module N.

sub g) The drive processor also takes care of the switching of the audio and video signals e.g. the muting of the signals during search actions.

sub h) The diagnostic software has been integrated in the drive software in such a way that many of the tasks of the drive are checked for proper performance. If a fault is detected in the execution of a task, an error code is shown on the screen as video overlay (like the index information). The software program is very useful on behalf of service diagnosing. The working and the use of this diagnosis software will be dealt with extensively in the REPAIR METHOD description.

S– bus

In the VP415, communication between the control module (S) and the drive processor module (R) is via the S–BUS.

The S–BUS is a synchronous communication link intended for use between a LaserVision drive and a host controller. The bus is bi–directional with handshake and is byte serial.

Bus activity is not continuous but is confined to a 'window' occuring in each video field. The window is of 8msec duration in each 20msec field period. Communications may not extend beyond the limits of the window. Execution of commands will commence following the termination of a window.

Commands are allocated a priority order:

Priority 1 More than one command may be sent during a window but only the last one accepted will be executed.

Priority 2 As for priority 1 but if a priority 1 command is included the priority 2 command will be ignored.

Priority 3 These commands will always be executed.

Constraints on operation

For the S–BUS to operate, the video from the disc must be locked to either the internal or an external reference in both line and field. Also the Manchester codes must be readable.

Command and response structure

The data is organised as packets each consisting of a three byte string.
A command from controller to drive processor module consists of 1 packet.
Responses may have a length of 0 to 5 packets, the length of a response being defined by a command from the controller in the form of – 05 00 0x where x is the number of packets required in the response. In the VP415 the initialising sequence calls for 4 packets.

By way of example the contents of these packets are :

Packet 1 Manchester code from line 18.
Packet 2 Byte 1 Disc loaded – CAV/CLV.
Byte 2 Player mode.
Byte 3 Error status.
Packet 3 Manchester code from line 16.
Packet 4 Byte 1 Laservision deck status.
Byte 2 Audio/video status.
Byte 3 Miscellaneous status.
If the fifth packet is requested this will contain the Manchester code from line 17.
In the case of the packets containing Manchester code information all zero's will be returned if the Manchester codes are not readable.

S–bus signals

Databus:

SD0–7	SD7 is MSB.

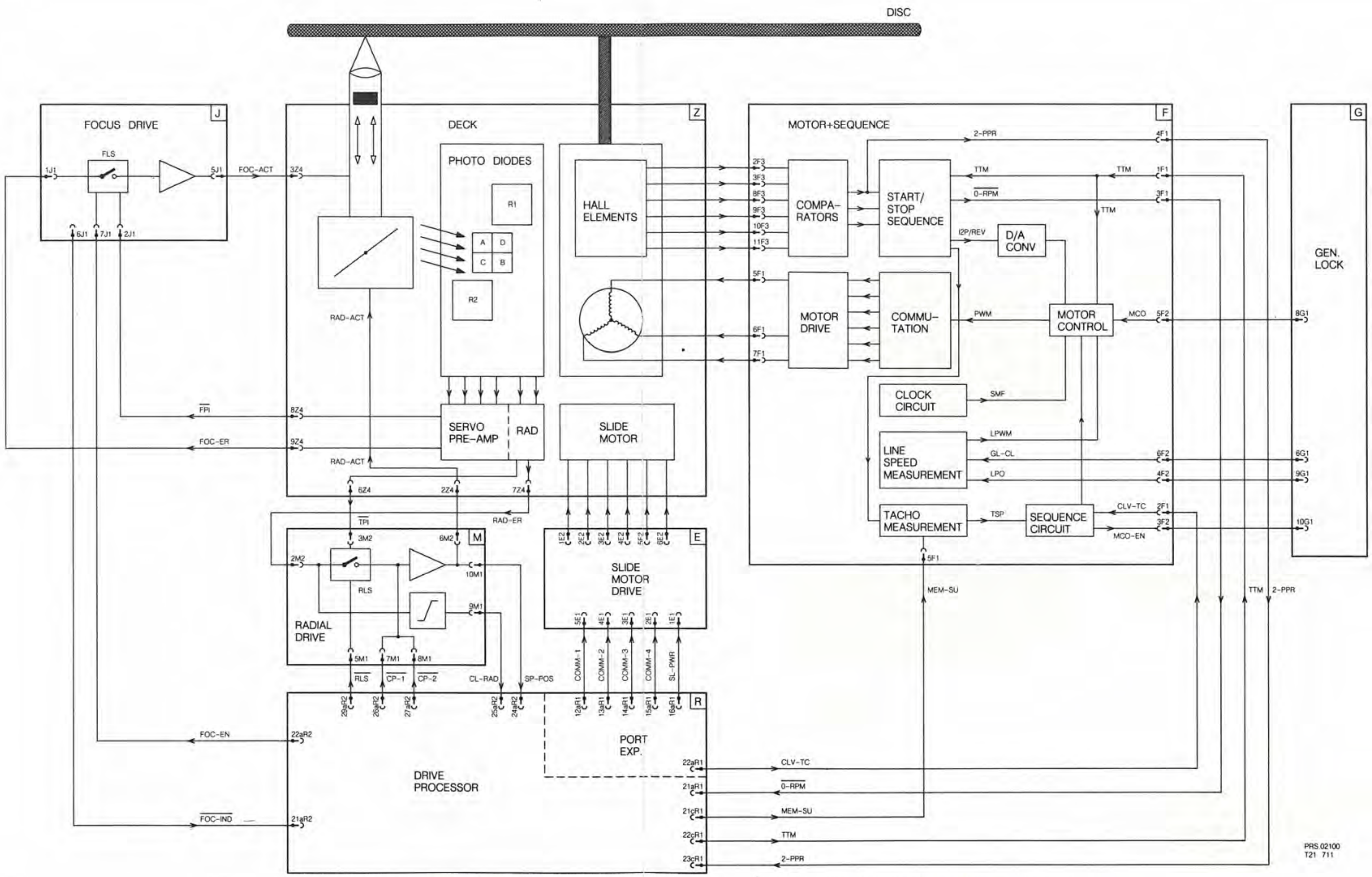
Signals to LaserVision drive:

WREN	Write enable (Write data to drive).
RDEN	Read enable (Read data from drive).

Signals from LaserVision drive:

DAK	Data acknoledge (Data has been read by drive).
DAV	Data available.
WINDOW	Drive can communicate.

Fig. SE 1 BLOCKDIAGRAM SERVO



The servo block diagram

For the blockdiagram of the servo signals see Fig.SE1. This diagram is a survey of all modules which are necessary for a correct functioning of the optical deck.
The modules are:
- The deck electronics **Z**
- Focus module **J**
- Radial drive module **M**
- Drive processor **R**
- Slide motor drive **E**
- Motor + Sequence module **F**
- Genlock module **G**

Short description

From the laser source a beam of laser light is projected on photodiodes A–D and R1–R2 on the optical unit. The laser light is converted into electrical signals and applied to the servo preamplifier and the radial amplifier. From the servo preamplifier a signal $\overline{FPI}$ (objective focussed) and the focus error signal are fed to focus drive module J via connectors 8Z42J1 and 9Z4–1J1. In the focus drive module focus drive signal FOC–ACT is generated and fed back to the objective via 5J1–3Z4. This module can only operate when focus enable signal FOC–EN which is coming via 22aR2 7J1 from the drive processor is "H". When the objective is focussed, the focus indication signal $\overline{FOCIND}$ "L" is fed via 6J1–21aR2 to the drive processor R.

From the radial part of the servo preamplifier radial error signal RAD–ER is applied to radial drive module M via 7Z4–2M2 and tracking position indication signal $\overline{TPI}$ via 6Z4–3M2. The output of radial drive RAD–ACT, which is fed via 6M2–2Z4 to the deck, controls the radial mirror. The radial module only operates when radial loopswitch signal $\overline{RLS}$ coming from the drive processor is "L". In case of jumps over one or more tracks, a $\overline{CP1}$ or $\overline{CP2}$ "L" signal is coming from the drive processor via 26aR2–7M1 or 27aR28M1 and at the same time clipped radial signal CL–RAD is fed back to the drive processor.

The drive processor controls the start of the turntable motor by means of the TTM signal which is via 22cR1–1F1 fed to the motor and sequence module F and when the motor is running a 2PPR (2 pulses per revolution) signal is fed back via 4F1–23cR1.

The drive processor also controls the position of the slide. This is executed by the output expander which feeds 4 commutating signals via 12aR1–15aR1 to 5E1–2E1 and a slide power signal SLPWR via 16aR1–1E1 to the slide motor drive module E. In the slide motor drive module the commutating signals are converted into drive signals for the slide motor and via plugs 1E2–6E2 supplied to the deck.

Motor+sequence module F takes care of the drive of the turntable motor. For control of this motor various signals are used, depending on the conditions. For running condition the TTM signal is "H" and is fed to the block start/stop sequence. The start/stop sequence block also gets information from the Hall elements in the motor via plugs 2–11F3 and the comparator block. During acceleration only the TTM signal is operating and via the motor control block converted in a pulse width modulated signal PWM with a minimum duty–cycle. The PWM–signal controls the commutation block which is supplying 6 drive voltages to the three output stages in the motor drive block. The output stages are connected via plug 5–7F1 to the motor. When the motor reaches the speed of 1500 RPM, the acceleration is stopped by the D/A converter and the motor control is taken over by LPWM, a frequency control signal coming from the block line speed measurement. In this block the line frequency of the video signal on the disc is measured by means of LPO pulses supplied by the GENLOCK module via 9G1–4F2. After a short time, when the speed is within 5% of the correct speed, the motor control will be switched over to phase control. This is performed by the sequence circuit which then delivers the motor control enable signal MCO-EN and via the Genlock module and plug 8G1–5F2 the 15625 Hz dutycycle controlled MCO– signal is supplied to the motor control block. The motor control will be switched back to frequency control in case of search mode on a CLV disc. In that case the CLV–TC signal from the drive processor, fed via 22aR1–2F1 to the sequence circuit will be "H". In case there is a loss of focus during search, the drive processor delivers a MEM–SU signal via 22cR1–5F1, which activates a memory in the tachocircuit and the information of the last motor speed will be stored. As soon as focus is correct again, the motor will speed up to the original velocity.

MODULE A - AUDIO PROCESSOR

On this module the hf audio signal (time base corrected) will be split up and demodulated into the 2 possible lf audio signals. See block diagram in Fig.A1. Drop out correction takes place for both channels. On/off switching of one or both of the audio signals is possible on this module.
The hf audio signal, time base corrected, (HFATBC) comes from the ETBC B module (H). This signal is fed through 2 identical circuits for both audio channels. Only some values of the applied components differ because of the different subcarrier frequencies (audio-1:683kHz, audio-2:1066kHz). Only the circuit for audio 1 will be discussed.

Circuit description

The HFATBC signal(plug 1A2) goes, via bandpass filter L5007, to the demodulator IC6201-2A and is available, as demodulated audio, at the output, pin 16, of IC6201-2A. The audio signal goes, via a lowpass filter (50kHz) and emitter follower T6101, to the source of FET 6102. Normally this FET is conducting , so the audio signal goes, via amplifier circuit T6103, T6104 and T6105, to pin 9 of switch IC6201-2B. If audio 1 is wanted as output signal, pins 9 and 8 will be "connected" and the lf audio 1 signal is available at plug 3A1 (AUD1) which will lead to the analog I/O module (U).

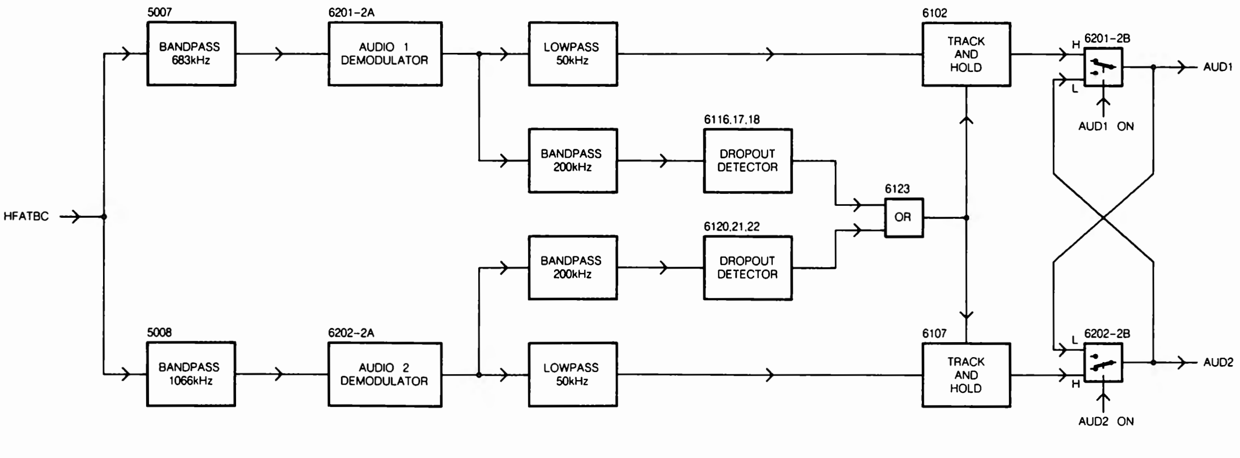
Drop-out correction

If a drop-out occurs in the hf audio signal FET 6102 will be switched off by a drop-out pulse on the gate of this FET. The voltage level on C2003 will be used as audio signal during that drop-out, thus avoiding "plops" (track and hold principle).
Drop-out detection takes place by monitoring the hf components remaining in the demodulated audio signal on output pin 16 of IC6201-2A. That signal will be fed through a bandpass filter (200kHz), realised with the RC components around T6115.
Detection is done with T6116, T6117 and T6118 and will create positive pulses in the case of drop-outs on the collector of T6118. The pulses are inverted by T6123 and will then drive the gate of FET 6102. If a drop-out is measured in the audio 1 channel, the track and hold circuit in the audio 2 channel is driven too.

Switching

Selection of the required audio channel is made with AUD1ON and AUD2ON. When only one channel is selected, both outputs are fed with that channel by means of cross coupling 2007, 3017 and 2021, 3041.

FIG.A1 AUDIO PROC. MODULE A



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MODULE B - RGB

See the block diagram in Fig.B1. The drop–out – and timebase corrected video, obtained from the VIDEO PROCESSING MODULE (C), is the input signal (CVBS) of this module. The CVBS signal will be split into a luminance and a chrominance signal and decoded into the R, G and B signals which are fed to the VIDEO MIXER MODULE (Y), via the ANALOG I/O MODULE (Ua). At the same time the luminance signal Y and the colour difference signals R–Y and B–Y are made available for creating the encoded CVBS signal on the ANALOG I/O MODULE (Ub).

Circuit description

First the incoming CVBS signal (plug 1B1) will be split into a luminance and a chrominance signal. By filtering the CVBS signal on the emitter of T7001, the luminance signal Y is present on the emitter of T7002 with an amplitude adjustable by potentiometer R3080. Via bandpass filtering with L5004 + C2005 the chrominance signal is present on pin 15 of IC7201.

Chroma decoding

The chroma signal will be decoded by IC7201, multistandard decoder, in an R–Y and a B–Y signal. The IC needs a crystal oscillator with a frequency of 8.86MHz (Cristal 5005) for chroma subcarrier generation. Capacitor C2010 is made switchable with T7012, driven by the CV/$\overline{CS}$ signal. The capacitor is connected to the +12V via the diode and resistor so that the AGC voltage remains at a fixed level if T7012 is out of conduction. The CV/$\overline{CS}$ signal will be low if the comp.sync signal is chosen instead of the video signal (mute function). In that case there will be no video content in the CVBS signal. The input signal, comp.-sync, has no burst so the gain control in IC7201 will give more amplification and can cause some problems. Therefore the AGC voltage will be kept of a high level.

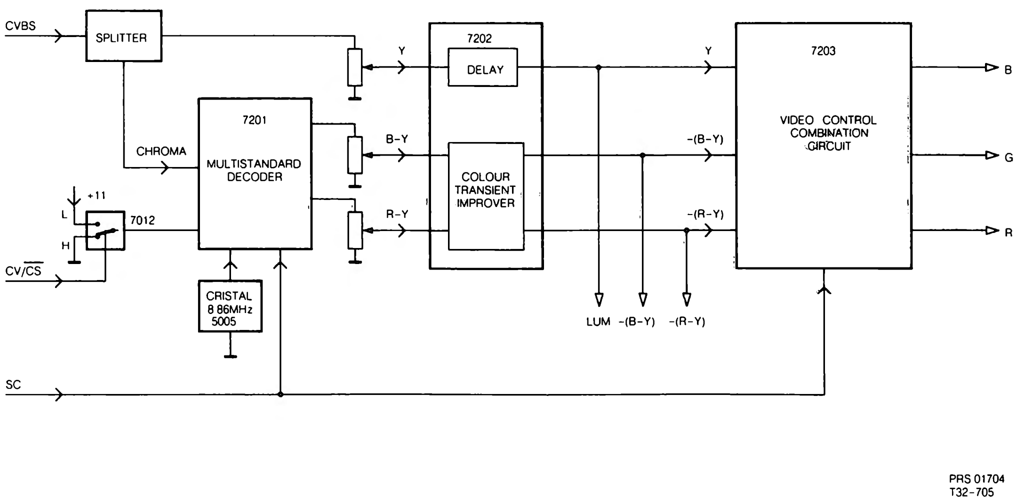
Colour transient improver

The colour difference signals R–Y and B–Y are present at pin 1 and pin 2 of IC7202 resp. This IC functions as colour transient improver. This means that the slope of the colour signal will be improved, thus giving a better visual impression.
The amplitudes of the (R–Y) and (B–Y) signals can be adjusted by potentiometers R3082 and R3084. The improved (R–Y) and (B–Y) signals are the output signals on pins 8 and 7 of IC7202.
Because of the processing time required to improve the colour transient, some time delay will occur in these output signals. The Y signal must have the same delay, which will be realised in IC7202. The output signals of IC7202 the luminance signal Y and the colour difference signals (R–Y) and (B–Y), will go to the ANALOG I/O MODULE Ub via plugs 10B3, 9B2 and 10B2 resp.

PAL decoder

At the same time the luminance and chrominance signals are going to IC7203, which takes care of decoding of these signals. The signals R, G and B go from pins 1, 3 and 5 of this IC7203, via output stages T7006, T7008 and T7010 to plugs 2B3, 3B3 and 4B3.
The dc–level of the output signals is adjustable by potentiometer R3045. The black level of the video signal is the reference point.

FIG.B1 RGB MODULE [B]



MODULE C - VIDEO PROCESSING

See block diagram in Fig.C1. On the video processing module switching is made possible between internal video (CV–TBC), external video (CV–EXT) and composite sync depending on the demands. Composite sync can only be used in the case of internal video selection (video from the disc). Composite sync is necessary if the player is in "pause" or during "goto" actions. The index frame and index characters can be inserted in the video signal, if wanted. Sandcastle pulse generation takes place for RGB handling and clamp pulses are created for black–level clamping. Clamping of the video is necessary to enable insertion of the index information.

Circuit description

Switching

The CV–TBC signal (timebase corrected video) arrives on this module at plug 3C1 (from ETBC–B module H) and goes via C2001 to switch IC7201–3A. This switch is controlled by the CV/$\overline{CS}$ signal of the DRIVE PROCESSOR MODULE (R). This signal can turn over the switch between video and comp.sync. This comp.sync signal is the output signal of switch IC7201–3C which is controlled by the CSREF signal, obtained from the REF SOURCE MODULE (D). That signal takes care of the switch–over at the right time between 2 dc voltages, 4V at pin 5 of IC7201–3C (video level) and 3.3V at pin 3 of this IC (top sync level). So a comp.sync signal is created for a.o.th. the sandcastle generator.
The output signal of switch IC7201–3A (pin 14) goes to pin 2 of switch IC7201–3B. This switch is controlled by the CV–E/$\overline{I}$ signal from the DRIVE PROCESSOR MODULE (R) to select internal or external video.
The external video comes from the ANALOG I/O MODULE (U) and is available on plug 9C2 and goes via a 2x amplifier circuit (T7001 and T7002), to pin 1 of switch IC7201–3B. The output signal of this switch goes via emitter follower T7003 to the base of T7008. The black level of this video signal is clamped at 4V via T7004, of which the gate is driven by clamp pulses, created in IC7202 with the aid of some external components.

Index insert

The video signal will obtain insertion of a grey level in the following circuit to get the index frame. This background level is realised by the $\overline{VOBN}$ signal at plug 5C1, coming from the DRIVE PROCESSOR MODULE (R). This TTL signal switches between 0V and 5V and goes, via T7005, to the base of T7007. The insert is via the collector of T7007, on the emitter of T7008. Via emitter follower T7009, the video signal including the background is present on the emitter of T7009. At this point the index characters will be inserted. The index characters arrive at plug 6C1 as VOW signal from the DRIVE PROCESSOR MODULE (R) . This signal is also switching between 0V and 5V and goes, via T7010 and T7011 to the base of T7012. In this circuit the character information will be made to the right voltage level, suitable to be inserted on the emitter of T7009 (characters at white level).
So on the emitter of T7009 the video signal, including index background and characters, is available.

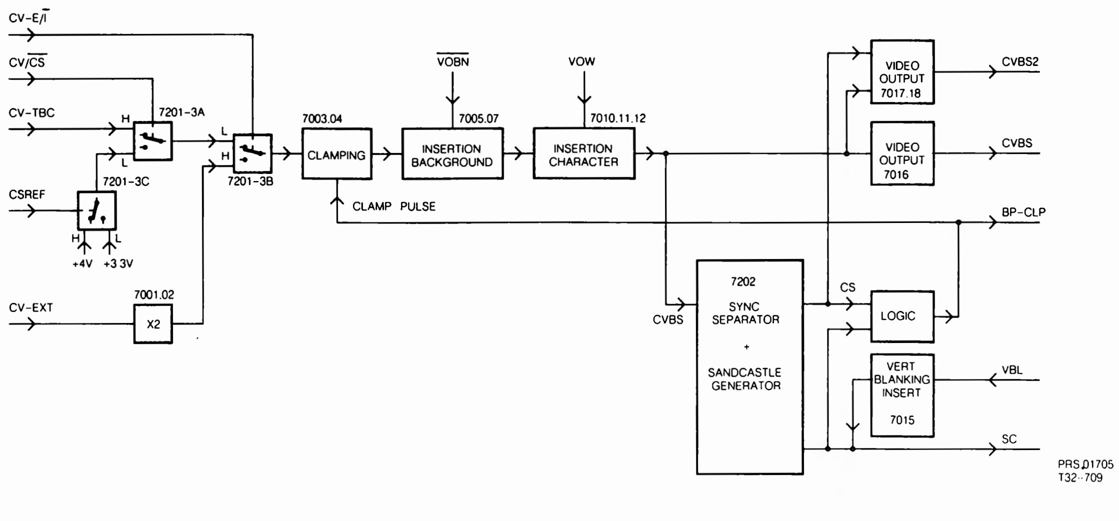
Video output

The CVBS signal on the emitter of T7009 goes, via T7016 and plug 1C2, to the RGB MODULE (B). This signal still contains the special burst signal, situated in the sync pulses. The ANALOG I/O MODULE needs the video signal too, but without the special burst signal. That signal is filtered out via T7017 and C2026, so via emitter follower T7018 the CVBS–2 signal (without special burst) is available at plug 6C2. FET T7017 is driven by the comp.sync pulse from IC7202.

Sync separator + sandcastle generator

The composite sync signal is separated from the video signal in IC7202. The comp.sync signal suppresses via an OR circuit, realised by a few diodes and via nand gate 7203–4D the clamp pulses during vertical sync. The signal for creating the clamp pulses is the burstkey pulse which is separated from the sandcastle signal of pin 6 of IC7202, via T7014. The clamp pulses are needed for clamping of the black level of the video signal.
The sandcastle signal contains line frequency parts and frame frequency parts. The line frequency part is created in IC7202, output signal of pin 6. The frame frequency part (VBL signal) is added to it via T7015. The sandcastle signal can be adjusted to the correct horizontal frequency (15625Hz) with potmeter R3035.
In IC7202 a square waveform signal (15625Hz) is generated, duty– cycle 50%, and is available on pin 4. With the aid of circuit IC7203–4A,–4B and –4C a duty–cycle control of the block signal is made possible. See the timing diagram in Fig.C2. The output signal of this circuit is fed back to IC7202 (pin 2) and takes care of the horizontal blanking duration in the sandcastle signal. The width of the horizontal blanking is adjustable with potmeter R3045.

FIG.C1 VIDEO PROC. MODULE C



MODULE D - REFERENCE SOURCE

The circuit on this module takes care of the generation of video timing signals necessary in the player. See block diagram in Fig.D1. These reference signals have to be very accurate in frequency and timing. There are three modes of operation:

1) Stand alone.
In this mode the 5MHz crystal is locked to the 10MHz crystal oscillator.

2) Composite sync external (CS–EXT).
In this mode the 5MHz crystal is locked to the signal CS–EXT.

3) Non standard composite sync (NS–CS).
In this mode the 5MHz crystal is locked to the signal NS–CS, coming out of the sandwich part via the analog I/O module U.

If no sync signals are provided in modes 2 or 3, the stand alone mode will function automatically.

Circuit description

ad 1) The 5MHz crystal 5001 is locked to the 10MHz crystal 5002. Inputs 8D2 and 4D2 are high impedance. In this mode the devices in use are: 5002, 7059–2A, 7060–4A, 7061–2B, 7062–3A, 7061–2A.

ad 2) The 5MHz crystal 5001 is locked to CS–EXT (8D2). For this mode the select signal CS–S/$\overline{NS}$ is at +5V. In this mode the devices in use are: 7050,51,52,53,54,55,56,57 and 7068.

ad 3) The 5MHz crystal 5001 is locked to NS–CS (10D1), coming out of the sandwich part. This mode is selected if CS–S/$\overline{NS}$ is pulled to ground. In this case 7068 is in use.

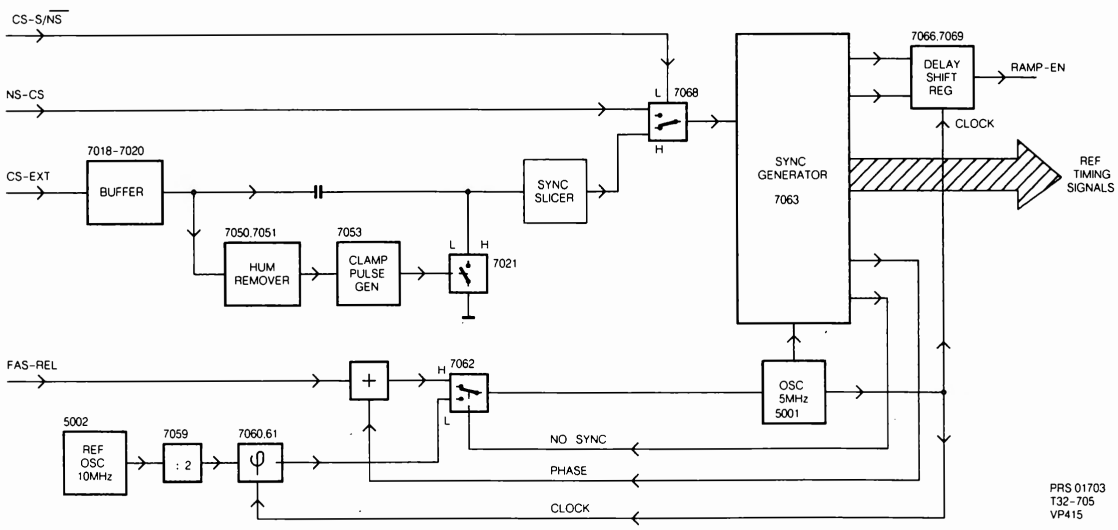
The NS–CS signal comes via the analog I/O module (Ua) from the vid mix module (Y). The CS–EXT signal can be applied directly to the analog I/O module (Ua). The control signal CS–S/$\overline{NS}$ can drive a switch circuit to pass the NS–CS signal or the CS–EXT signal. This control signal comes from the VID MIX MODULE (Y) and will be available on this module via the analog I/O module (Ua). The switch circuit is realized with the aid of 3 NAND gates in IC7068.

If neither comp. sync signal is available, it will be detected by the sync generator IC7063 which creates the "no sync" signal at output pin 13 in that case. The no sync signal takes care of the functioning of the reference oscillator of 10MHz by driving switch IC7062–3A.
The CS–EXT signal can be a clean comp. sync signal or a complete CVBS signal. In case of a CVBS signal a sync slicer circuit (IC7054–7057) will derive a comp. sync signal from that signal. Fixing of the dc level of the external sync signal is also necessary. Therefore the signal goes via a "HUM remover" circuit (IC7050,7051) to remove the video content of the complete signal. The result is a clean comp. sync signal which takes care of triggering of a clamp pulse generator circuit (IC7053). This circuit creates pulses for clamping of the signal offered to the sync slicer, by switching FET T7021.

The sync signal input of the sync generator IC7063 can be seen as a "master" input to have the outputs related in phase. Phase comparison takes place in IC7063 and depending on the result an output signal PHASE is realised controlling the varicap (6013) voltage of the 5MHz oscillator.
An FAS–REL signal is provided to this module. This signal is created on the analog I/O module (Ua) and is a dc voltage adjustable between 0V and 8V with potmeter R3149 on module Ua. This signal can influence the horizontal shift of the outgoing video signal. So the video signal of the player can be related to a possible computer video signal. The control range is from +4us (0V) to –4us (8V).
See for greater detail of the timing the data sheet for the SAA1043.

Because of the necessary processing time of the video signal in the sandwich part, an equal delay time has to be realised in the player part. This is done with the variable length shift registers IC7066 and IC7069. The delay time created in IC7069 is determined by the address offered to this IC. The required address in case of the PAL system is mentioned in the table on the circuit diagram.

FIG.D1 REF SOURCE MODULE D



Output signals:

FI field identification for genlock

RAMP–EN ramp enable signal to ETBC–C module for phase measurement in tangential error circuit

80–FH 80–FH = 1.25MHz signal to analog I/O module, not used in the VP415

TXT–WH teletext window horizontal to analog I/O module for txt insertion in the correct line

400HZPAL to analog I/O module (Ub), not used in the VP415

TXT–WV teletext window vertical to analog I/O module for txt insertion in the correct line. This signal is identical with REFV.

REFH horizontal reference signal, to drive proc.module (R) for hor. sync character insert, to the genlock module (G), and the analog I/O module (Ua) for loop through to the vid mix module (Y)

REFV vertical reference signal, to drive proc.module (R) for vertical sync character insert and VBL generation. This signal is identical with TXT–WV.

CBL composite blanking signal, to analog I/O module (U) for loop through to the vid mix module (Y) and is used for blanking

CS–REF composite sync reference signal to analog I/O module (Ua) and the video processor module (C)

CLP clamp pulse to analog I/O module

H/2 PAL 8kHz pulse to analog I/O module (Ub) for 0°–180° phase switching of the chroma subcarrier for R–Y

BF burst flag signal to the analog I/O module

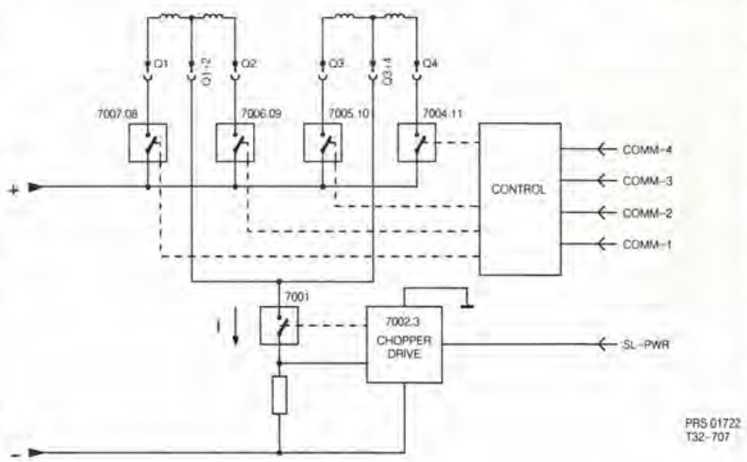
MODULE E – SLIDE DRIVE

The slide drive module, see the block diagram in Fig.E1, controls the slide drive motor. The function of the slide drive motor is to move the LDU under the disc in such a way that the tracks can be read out in an optimal way.

Circuit description

The slide is driven by a stepping motor. Each step moves the slide by about 50 track spaces. The motor is driven by means of pulses on COMM 1–4 and SL–PWR which switches the motor coils between holding and moving power levels via an astable multivibrator with transistors 7002, 7003.
The drive signals are provided by the drive processor, module R.

Fig.E1 SLIDE DRIVE MODULE E



MODULE F – MOTOR + SEQUENCE

The circuits in this module take care of the drive of the turntable motor. See servo block diagram and block diagram in Fig.F1.
The turntable motor is of the brushless type provided with Hall elements. The main groups on the board are:

–The MDS–IC 7202. This IC takes care of the communication between the motor and other circuits and delivers the required drive voltages to the output amplifiers of the motor.
–The Hall elements which are continuously passing the position of the motor via comparators to the MDS–IC.
–The logic circuits around transistors 7020–7022 which are controlling the motor with regard to the several conditions like start, brake, motor control and current limiting.
–The pulsewidth modulator IC 7230 which is converting the drive voltages into a duty cycle controlled input pulse for the MDS–IC
–The output stages which are supplying the required drive currents to the motor coils. This currents are derived from the commutating voltages supplied by the MDS–IC.

Circuit description

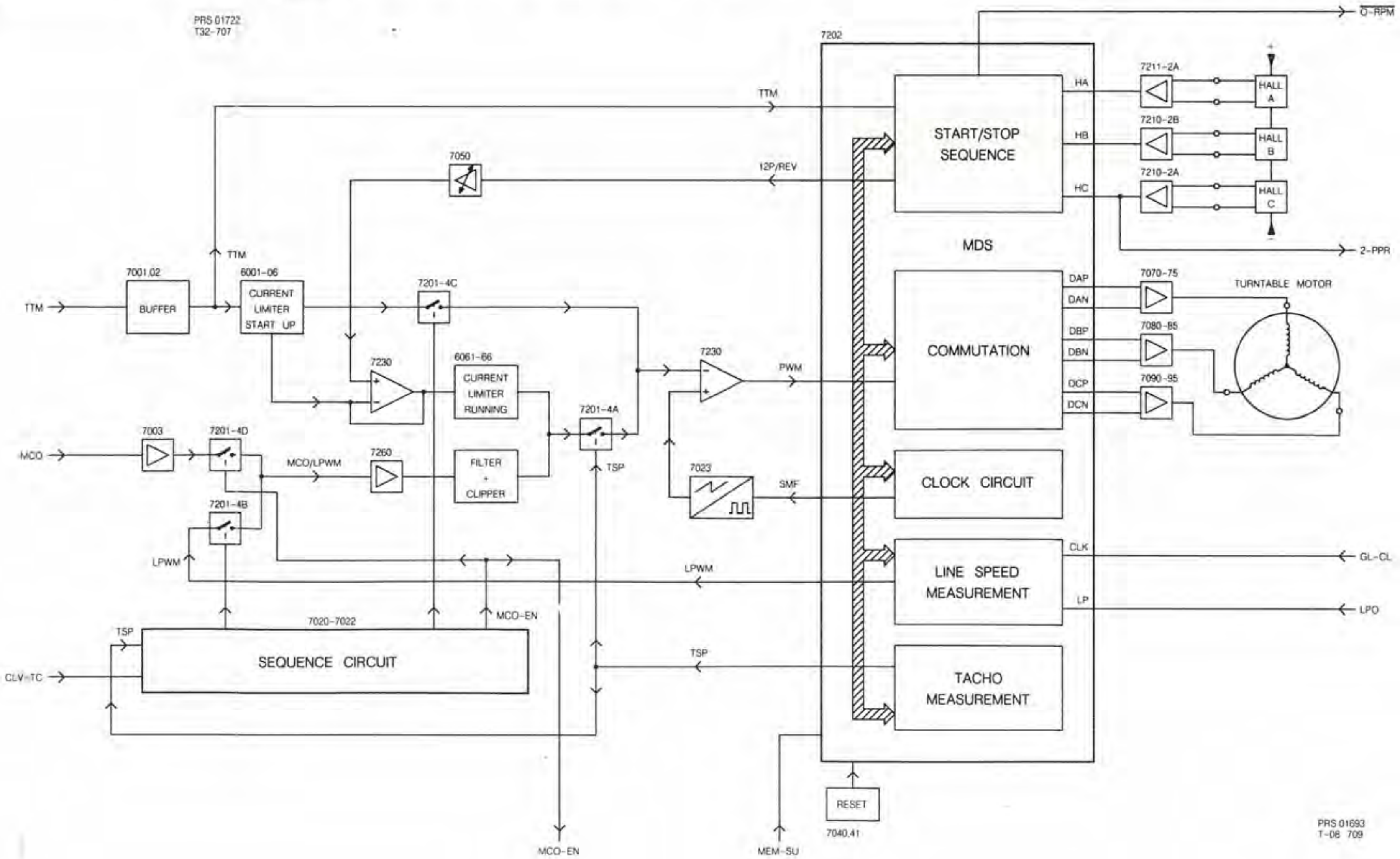
For a proper functioning of the turntable motor, several input signals are required:

–TTM, the turntable motor on signal which is "H" during start and play conditions and delivered by the drive processor.
–MCO, a duty cycle controlled pulse which is originating from the GenLock Module and only active in the locked position.
–CLV–TC, a logic "H" signal, present during track crossing at CLV discs.
–MEM–SU, Memory start up, a logic "H" signal in case of focus loss on CLV disc in search mode. The last tacho information is then stored in a memory.

Start condition

In start condition the TTM signal is "H" and is via the buffer amplifiers 7001–7002 fed to the MDS–IC. As long as the motorspeed is below 1500 RPM, the output signal TSP of the tacho circuit in the MDS–IC is "L" which causes switch 7201–4D to be open. The TSP signal is also fed to the sequence circuit and causes that 7021 is blocked. The collector voltage is then "H" and switch 7201–4C is closed. The "H" voltage from TTM is fed via 7201–4C to pulsewidth modulator 7230–2A. This results in a low duty cycle and causes speeding up of the motor. The charge current of 2031 is limited by the diodes 6001–6002. The pulsewidth modulator 7230–2A compares the control voltage with a sawtooth signal derived from the clock circuit in IC 7202. The frequency is about 17.6 kHz. The sawtooth shaped voltage is obtained by the generator consisting of transistor 7023, capacitor 2030 and the resistors 3029–3031. It will be clear, that the the duty cycle decreases when the d.c. control voltage increases.

Fig.F1 MOTOR+SEQUENCE MODULE F



Running condition

As soon as the motor is running, 12 p/rev. pulses are applied from 30IC–7202 to the base of transistor 7050. This causes the input voltage on 5–IC7230 to increase from about 2.7V up to 3.2V. After the opamp and the diodes 6061–6066 a small part of the output voltage is fed to switch 7201–4D. As soon as 1500 RPM is reached, the TSP–signal becomes "H" and switch 7201–4D will close. At the same time transistor 7021 starts conducting and switch 7201–4C will open. This means a lower input voltage at the pulse width modulator and the motor will not accelerate anymore.

Frequency control

When the motor has reached a speed of 1500 RPM and TSP is "H", switch 7201–4B is closed via resistor 3021 and diode 6022. Now the motor control will take place with the aid of the LWPM signal and the phase compensation network IC 7260–2B. The output will be combined with the running current limiter signal.

Phase control

In running condition TSP has become "H", capacitor 2020 is charged and after about 0.5 sec transistor 7020 starts conducting and the collector voltage will drop. Switch 7201–4B opens and there is no frequency control anymore. At the same time transistor 7022 is blocked and due to the high collector voltage, switch 7201–4A is closed. From this moment on MCO–EN becomes also "H" and the motor control is taken over by the MCO–signal.
In case of CLV–track crossing, which occurs in CLV–search mode, the CLV–TC–signal becomes "H", which means that there is only frequency control by the LPWM–signal.

Active braking

When TTM becomes "L", TSP is "L" too. Switch 7201–4A will open and 7201–4C will close. A lower voltage is now given to the pulsewidth modulator input. Upon motor stop, all driver inputs are disabled.

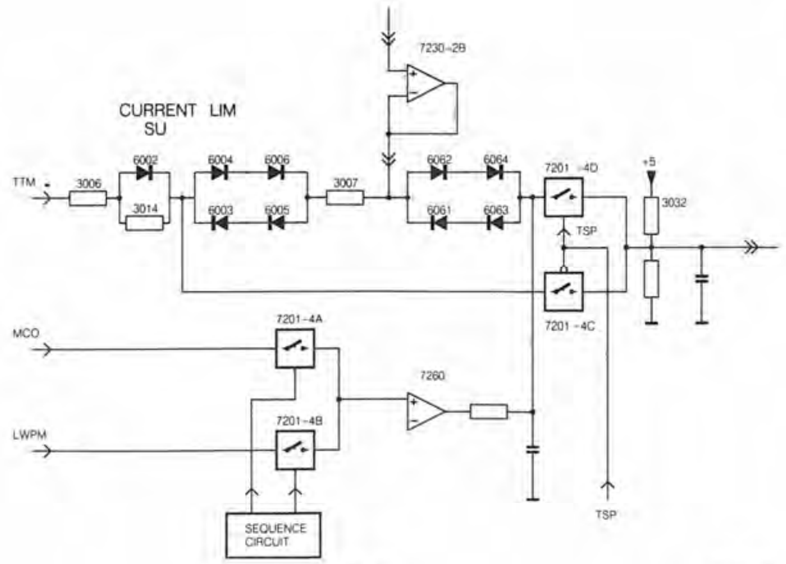
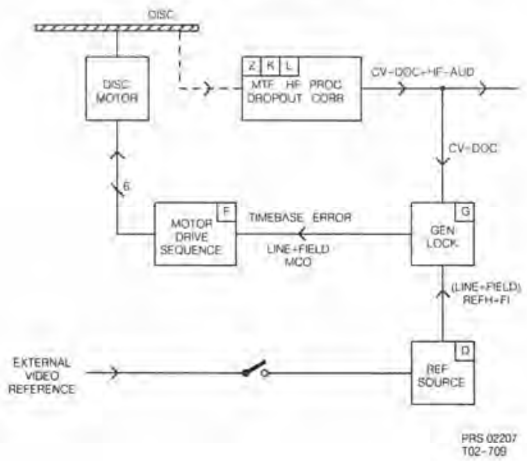


Fig F2

MODULE G – GENLOCK

The purpose of this module is to establish lock in both frame and line between the disc and the sync generator on the reference source module (D). Thanks to the fact that the player is equipped with RGB, synchronization of the colour subcarrier is not required. Locking is possible at the internal sync generator which is highly accurate. In this way it is possible to place, before the disc is turning, text on the screen which is coupled to a sync to which the disc will also be synchronized later. Moreover, the video signal of the disc can be synchronized to an external video or sync signal. See the block diagram in Fig. G1. Locking is done by adapting the rotational speed of the disc or the motor control via module F. In this way the phase of the read–out video (CV–DOC) is controlled.
The time required by the player for synchronization can be divided into two parts. First the internal sync generator should synchronize to the external signal. This can take maximum 7 s. However, this action can already be started when the disc is still standing still. Next the disc should synchronize to the internal sync generator. This may take 3 s. When the phase of the external sync is reset arbitrarily during the program, the internal sync generator should fall into step and the disc should again lock to the internal sync. This may take a total of 7 s because both actions take place simultaneously.

FIG.G1 BLOCK DIAGRAM – GENLOCK



Circuit description

For the blockdiagram of the genlock module, see Fig.G2. Sync separator IC 7205 runs on a VCO with a centre frequency of 4.5MHz and control element varicap diode 6014.

IC 7205 outputs:

20	LPO	Line pulse out, a line sync pulse obtained from input signal CV–DOC (Composite video dropout corrected).
19	M–LOCK	CV–DOC/VCO locked.
15	MCO	Motor control out, duty cycle proportional to speed error.
4	DEM–BK	Burst key pulse from demodulated video '(CV–DOC).
8		Frame pulse.
3		4.5MHz clock.
6		Composite syncs derived from CV–DOC.

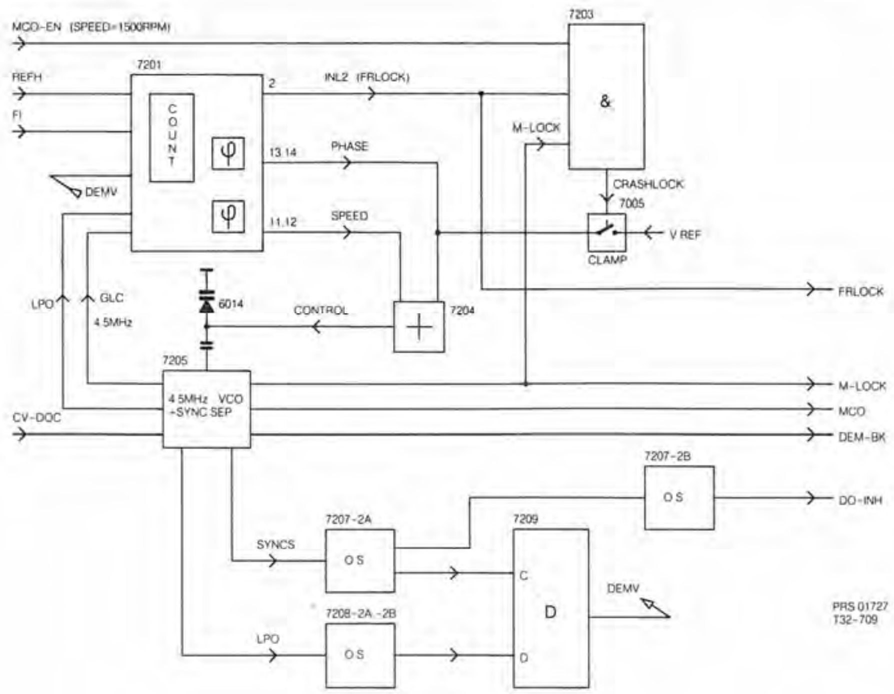
In IC 7205 the phase comparison between the line pulses of the disc (derived from CV–DOC) and the line frequency pulses of the reference (4.5 MHz divided by 288) takes place. The phase difference will cause a change in the duty cycle of the MCO signal. The MCO signal is the input signal for the motor control. The line pulses of the disc are thus phase–coupled to the reference.
The signals from pins 4,6 and 8 are combined (IC 7206–2B, T 7018) to give DEM–BK. The pulses are suppressed around the vertical sync pulse.
The signal from pin 8 is stretched in one shots 7207–2A, 7207–2B to give DO–INH (dropout inhibit during the lines occupied by the Manchester codes).

Establishing lock

Lock is established in speed and phase by adjusting the voltage applied to varicap diode 6014. This occurs in defined stages. During lock–in (crash lock) the phase control (outputs 13,14 IC 7201) is disabled by:
a) MCO–EN until 1500 rpm is reached, and
b) Line and frame lock has been achieved (INL2, pin 1,IC7201).
When this stage is reached MCO–EN and INL2 indicate "OK" and via ICs 7203–4B, 7203–4C and transistors 7004, 7005 the clamp voltage is removed from the phase correction network consisting of transistors 7006, 7007 and IC 7204–2A. Phase control outputs 13 and 14 of IC 7201 are now effective. Dependent on the required phase correction the charge on capacitor 2008 will be changed by charging more via transistor 7006 or discharging more via transistor 7007. The changing charge on capacitor 2008 will via OPAMP ICs 7204–2A and 7204–2B adapt the varicap voltage on diode 6014 and thus the reference frequency of IC 7205.

IC 7201 operates by comparing FI (field identification) and REFH from the reference module (D) with LPO and DEMV (obtained from CV–DOC in IC 7205).
The comparison is obtained by counting GLC pulses.
Speed corrections are made in a decreasing series of steps, from +/– 1.8% to +/– 0.1%. The dividend of the variable divider is dependent on the number of line pulses which is counted between the leading edges of the field identification of the disc (DEMV) and the field identification of the reference (FI). When the phase difference is maximum the disc goes with a speed of 1.8% relative to the nominal to the reference. As the phase difference decreases, the relative speed decreases too. In this way frame lock is realized. The next action is the synchronization of the line pulse. If genlock IC 7201 establishes that there no longer are line pulses between the field identification pulses of the disc video and the reference, the FRLOCK signal becomes active (high level, 5V). This is followed by permament comparison between the line pulses of the disc and the line pulses of the reference.

Fig.G2 GENLOCK MODULE G



MODULE H - ETBC B

This module is part of the electronic timebase correction system (see block diagram overall timebase correction, fig.H1).
It is comprised of two CCD (charge coupled devices) delay lines to effect coarse correction (+/- 17 micro secs) and two variable LC delay lines to effect fine correction (+/- 50 nano secs).
Video and audio signals are treated separately, in parallel. IC 7201 is the CCD for the video channel and IC 7203 the CCD for the audio channel (see fig.H2).

On this module the timebase of the drop-out corrected composite video (CV-DOC) is corrected. This is necessary because of the presence of several tolerances (disc, centring, motor) which cause variations on the line phase of the video signal read. The variations can be about +/- 17us compared with the reference. This is unacceptable for video processing, so correction is needed. In the previous players the correction was realised in a mechanical way, the tangential mirror. In the new-generation disc drives the tangential mirror is not applied anymore. The timebase is corrected electronically. The ETBC B module will have the timebase corrected comp. video signal (CV-TBC) as output signal for further processing on the vid proc module (C).
Also it is necessary to have timebase correction of the audio signal (HFAUD), which is realised too on this module. As result the output signal is the timebase corrected hf audio signal (HFATBC).

Control of the time delay is by means of TANG-ER and BURST-ER both from the ETBC C module (I).

Circuit description

Video timebase correction

The CV-DOC signal from the video do corr module (L) arrives at this module on plug 2H2 and goes, via emitter follower T7013 and a lowpass filter (≤6.6MHz), to the input of the CCD memory IC 7201. Lowpass filtering is necessary to prevent aliasing effects in the CCD. The video signal will get a time delay in the CCD depending on the frequency of the clock signal offered. The clock oscillator is connected to pin 14 of IC 7201 and functions as a voltage controlled oscillator (VCO), IC 7206. The voltage offered is the measured error signal (TANG-ER) created on the ETBC C module (I). The TANG-ER signal is present on plug 4H1 of this module. As the clock rate is determined by TANG-ER, so the time the signal is delayed in the CCD's is also determined by TANG-ER. This shows that as TANG-ER is a measure of the time error, a loop is set up which will compensate for timebase errors within the measuring accuracy of TANG-ER.
The frequency of the clock oscillator output signal is inversely proportional to TANG-ER and has a centre frequency of about 19MHz.

Referring to the anti aliasing phenomenon mentioned above it will be seen that low pass filtering of the input signal is required to eliminate any frequencies greater than half the clock rate.
In the CCD IC 7201 a flipflop is situated which acts as a :2 divider. The 2 output signals of this flipflop go to the 2 x 680 stages shift register, so the complete delay is 1360 stages for the video signal (see fig.H2). Reading by the CCD memory happens every positive going edge of the flipflop output signals Q and $\overline{Q}$. For the timing of the internal flipflop, see Fig.H3.

FIG.H1 BLOCK DIAGRAM - OVERALL TIMEBASE CORRECTION

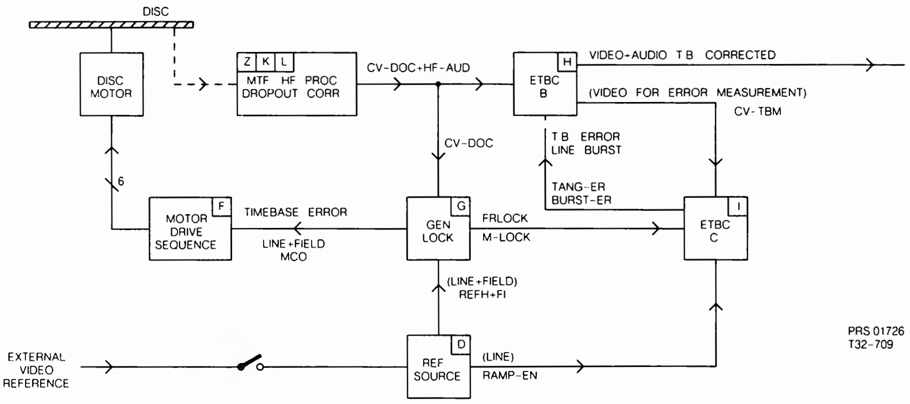
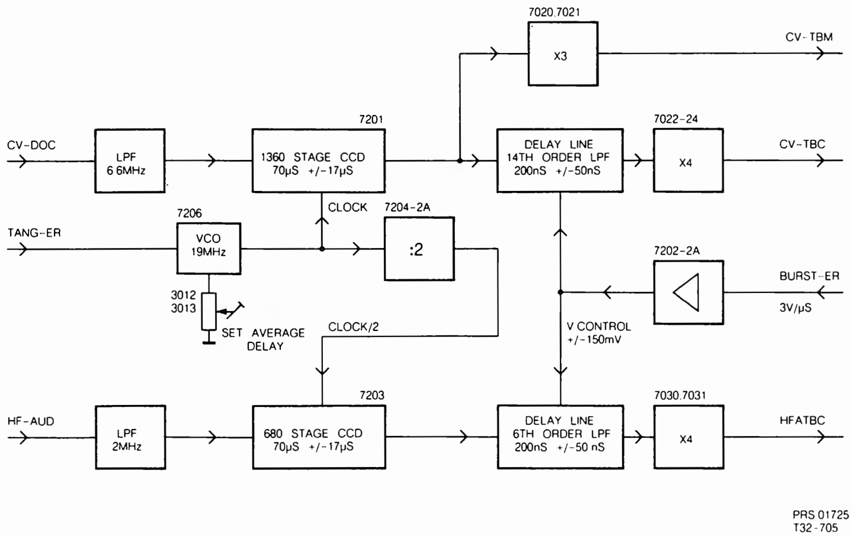


FIG.H2 ETBC B MODULE H



The timebase corrected output signal of IC 7201 goes, via T7018, to T7020 to have a 3x amplification. The signal continues from the collector of T7020, via emitter follower T7021, to plug 7H1 as CV–TBM signal. For the system this signal is the measuring signal to create the error signals on the ETBC C module (I). On that module a comparison takes place of the measure signal and the reference signals. So this is the feedback loop of the timebase correction mechanism.
At the same time the signal of the emitter of T7018 goes, via T7017, to a steep lowpass filter (≤7MHz). This filter is realised by coils L5002.....L5008 and the varicap diodes D6005.....D6010. The filter circuit provides the video signal with a delay time of 200ns and depending on the voltage on the varicap diodes another +/– 50ns. This depends on the BURST–ER signal. Lowpass filtering is also necessary to prevent switching noise of the CCD.
In the video path there is some high frequency loss in the CCD. This is compensated for with a high pass network in the emitter of T7022 giving a rising response of about 6dB between 2 and 4MHz. From this network the video signal will be available on plug 2H1 as CV–TBC signal, via amplifier T7023 and emitter follower T7024.
The BURST–ER signal is present on plug 5H1 and goes, via potentiometer R3134, to the + input of opamp IC 7202–2A. From the output of this opamp the signal goes, via voltage follower IC7202–2B, to the varicap diodes of the variable LC delay line.
Dependent on the voltage offered the delay time will change, and this with a maximum of the above-mentioned +/– 50ns. The functioning of this circuit can be seen as a fine correction of the timebase errors.

Audio timebase correction

The HF–AUD (high frequency audio) signal from the HF PROC module (K) arrives this module (H) on plug 1H2. The audio signal goes, just like the video signal, via a lowpass filter to a CCD memory IC (IC7203). The audio signal needs timebase correction too.
The clock drive for the shift register is driven by the clock signal coming from flipflop IC7204–2A. The input signal of the flipflop is realised by the same VCO as used for the video path.
The flipflop IC7204–2A is used as :2 divider. The clock frequency can be half the value because of the lower number of stages used (680 instead of 1360). The time delay will be the same as for video, but the passband of the audio signal is lower .

The output signal of CCD IC7203 goes, via emitter follower T7026, to a lowpass filter (≤2.3MHz) to filter the switching noise.
This LC filter functions also as variable delay line with the aid of the varicap diodes 6013. The varicap diodes are controlled by the BURST–ER signal. The output signal of IC7202–2A, derived from the BURST–ER signal, goes, via C2059, potentiometer R3122 and emitter follower T7029, to the varicap diodes. The controlled time delay differences will have the same value as for the video signal. Via amplifier stage T7030 and emitter follower T7031 the timebase corrected hf audio signal is available on plug 9H1 as HFATBC signal.

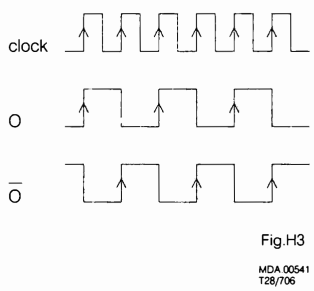


Fig.H3

MODULE I – ETBC C

This module is part of the electronic time base correction system (see block diagram overall timebase correction, fig.H1). Its primary function is to measure the timebase error and provide coarse (TANG–ER) and fine (BURST–ER) correction control signals to module H. To give the required accuracy, error measurement is made at two levels of precision.
The CV–TBM signal is coming from the ETBC–B module (H) and is the composite video signal for measuring the timebase error.
See Fig.I1 for the block diagram of this module.
Coarse measurement is obtained from comparison of syncs in CV–TBM and the RAMP–EN signal. The RAMP–EN signal is the reference timing signal from the REF SOURCE module (D). Fine error measurement is obtained from the special burst, a 3.75MHz signal during sync pulses. This inserted signal can only be found in the video signal from the disc.

Circuit description

Tangential error detector

For the circuit diagram of the tangential error detector, see Fig.I2.
CV–TBM applied to pin 9, IC 7203 (synchronization IC) is passed through an internal low pass filter and the syncs are separated. From these a line sync signal is obtained (HMANCH, pin 20 of IC 7203). From this signal a constant length pulse is obtained by one shot IC 7201–2A. In a similar way a pulse of the same duration is obtained from RAMP–EN (from module D). See the timing diagram in Fig. I3 (pulse width T1=33μs).

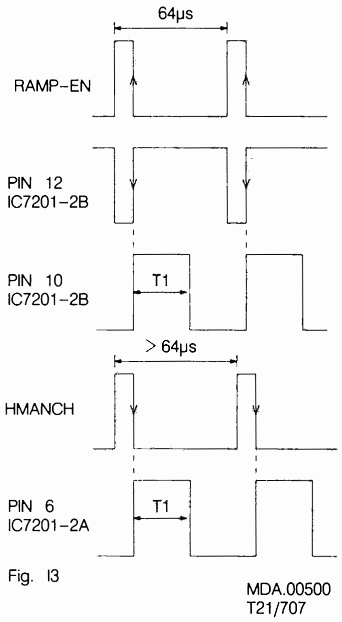


Fig. I3

Comparison of the relative timing of these signals in 7202–2A, 7202–2B, gives a current in one of the collectors of 7004, 7005 which is proportional to the time error. See the timing diagram in Fig.I4 (pulse width T2=4.7μs), assuming that the disc video and hence the HMANCH signal derived from it has a longer timebase than the reference (also see fig. I3). This may e.g. occur when the disc turns too slowly.

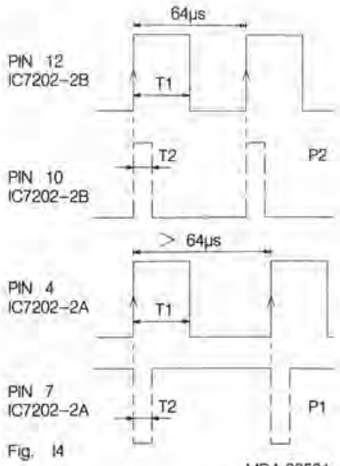


Fig. 14

MDA.00501
T21/706

In Fig.14 output pulses P1 and P2 are drawn with dotted lines because these signals are only present when clear input pins 3 and 13 resp. are "high" (C1 and C2). These inputs are not constantly high but dependent on the outputs of one shots IC 7201 -2A and -2B. See Fig.15 for the actual timing.

The timing figures show that a positive pulse remains (P2). Via T7005 it will see to a discharge of C2015. As a result the dc level of the TANG-ER signal will rise via buffering by IC 72072B. In this way adaptation of the timebase correction takes place, in the sense that the throughput time of the video signal is reduced.

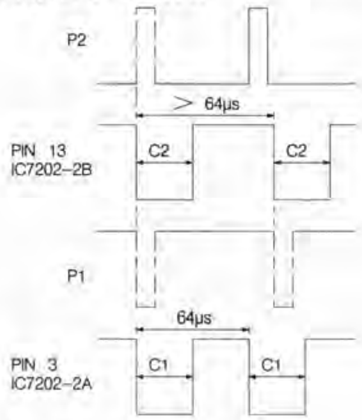


Fig. 15

MDA.00502
T21/706

C2015 will be charged for too short a period time of the disc video relative to the reference. Charging will take place by the negative pulses (P1) and T7004. The dc-level of the TANG-ER signal will drop. As a result the throughput time of the video on module H will be lengthened.

Special burst separator + gate

From CV-TBM the special burst is extracted by T7001, L5001, C2005, and is, via emitter follower T7002, available at the source of FET 7003. The special burst signal is gated by the syncs from pin 6, IC 7203 at T7003.
T7011, T7012 act as a 'special burst presence' detector, the collector of T7012 going high if a special burst is present.
The special burst is applied via T7029, T7014 to input 4, IC 7206-2A.

Sample detector

The sample detector, see Fig.16, sees to delivery of a sample pulse signal which is an accurate measure for the frequency of the disc video. This is realized by looking to exactly the same zero crossing of the special burst signal each line time.

The special burst signal is fed to one shot IC 7206-2A, pin 4. Pin 6 of this IC will change over to a high level as soon as pins 4 and 5 are high and pin 3, reset input, is high too. The latter will be realized via one shot IC 7206-2B and T7015. The input signal of this IC is the comp. sync signal derived from the disc video. This comp.sync signal thus triggers one shot IC 7206-2B, which delivers in its turn a defined pulse at pin 10. Via T6215 this pulse sets one shot IC 7206-2A free. Dependent on the pulse time at pin 3, which is determined by C2042 and R3081, one shot IC 7206-2A will be reset (low level at pin 3). One shot IC 7206-2A will be active after release at pin 3 and will give a pulse at pins 6 and 7 at the next zero crossing of the special burst signal. T7016 ensures the selection of the correct zero crossing with respect to the line sync.

Tangential phase detector

The RAMP-EN signal of REF SOURCE module D is tapped by means of resistors R3127 and R3128 and goes to the tangential phase detector circuit, see Fig.17. The RAMP- EN pulse goes to the base of T7027 which is incorporated in a one shot circuit, formed by T7027 and T7028. The output pulse of this one shot goes to the base of T7019 and will let this T7019 conduct at high level thus discharging C2052. The output signal of IC 7206-2A, pin 7, is via C2049 present on the collector of T7017 as sample pulse signal.
The sample pulse signal indicates exactly where a fixed zero crossing of the special burst signal is situated. The frequency of the sample pulse signal can be seen as an accurate measurement of the line frequency of the disc video signal. Via R3094 this pulse is present at the base of T7018 and will let this T7018 conduct in case of a low level. As a result C2052 will be charged via R3097. This causes a certain sawtooth signal on C2052. The total picture of charging and discharging can be seen in Fig.18.

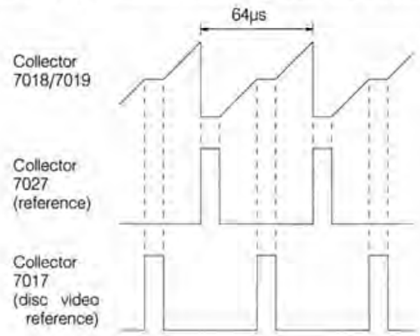
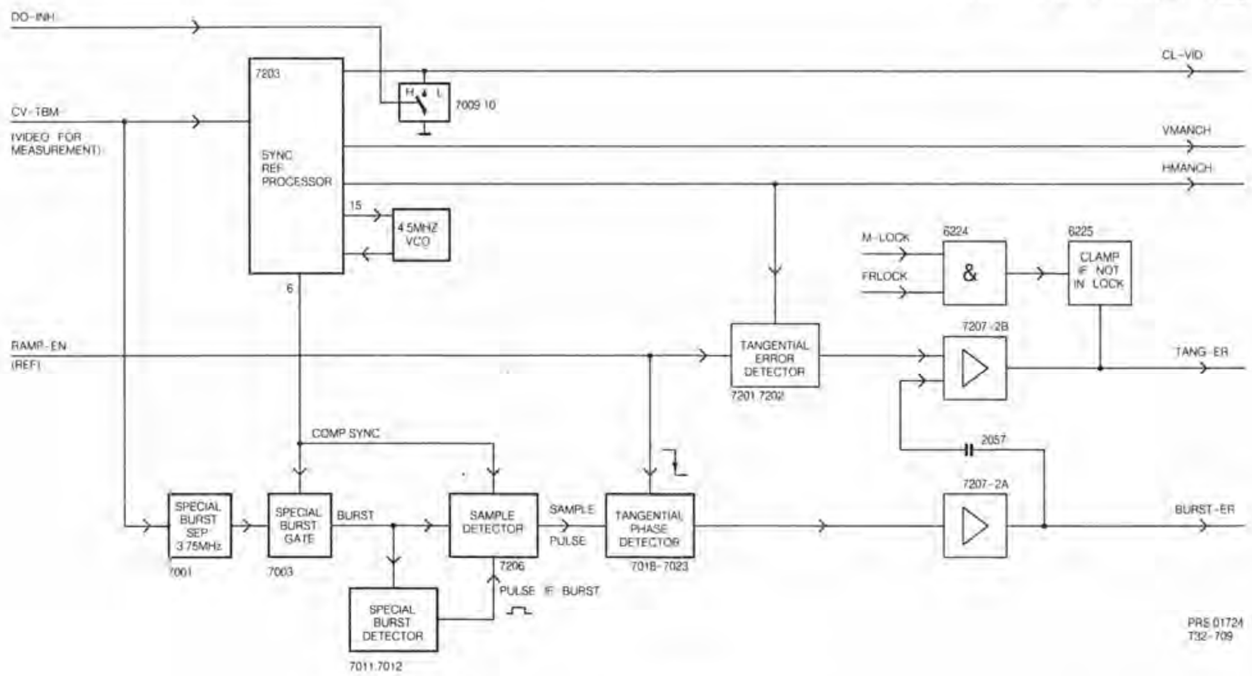


Fig. 18

MDA.00506
T21/703

This sawtooth signal goes via T7020, T7021 to the source of FET T7023. This FET T7023 sees to sampling out of the platform level in the sawtooth voltage. This voltage level will be present at C2053 then. When the zero crossing of the special burst takes place, T7023 is turned on loading a new voltage into C2053. The value across C2053 is proportional to the timebase error as measured from the special burst. Should the phase relation between the RAMP-EN signal and the sample pulse be disturbed, the result will be a level change of the platform in the sawtooth signal. Thus a dc-change at C2053 and thus, via opamp IC 7027-2A, a change in the BURST-ER signal.

FIG.11 ETBC C MODULE [I]



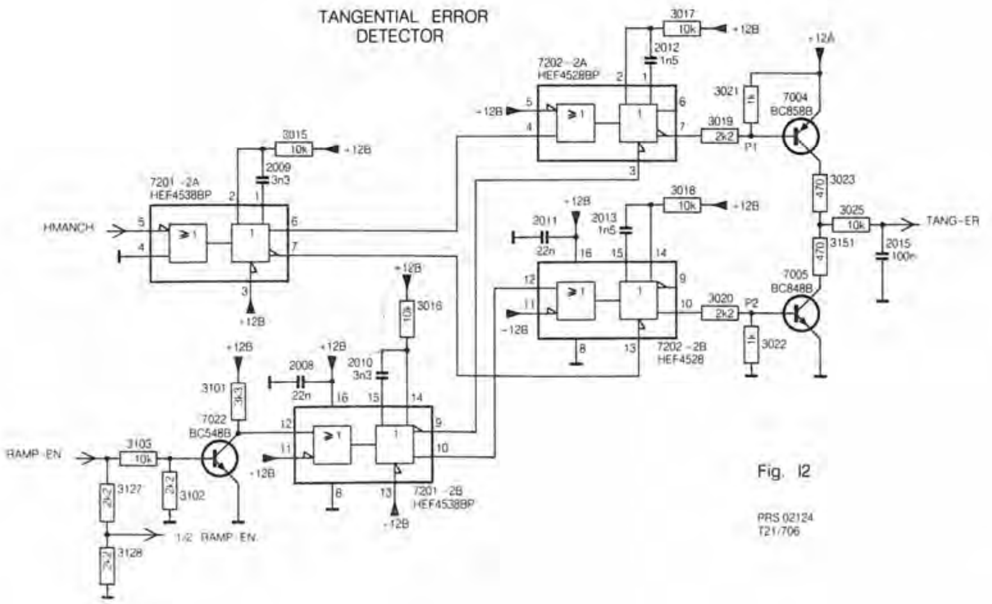


Fig. 12

PRS 02124
T21/706

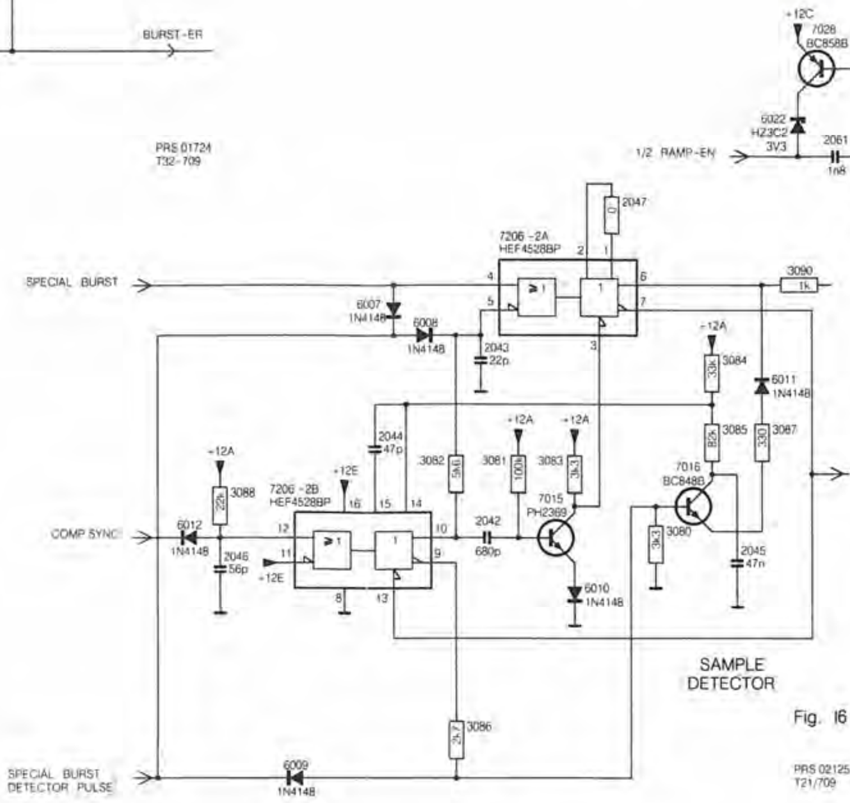


Fig. 16

PRS 02125
T21/709

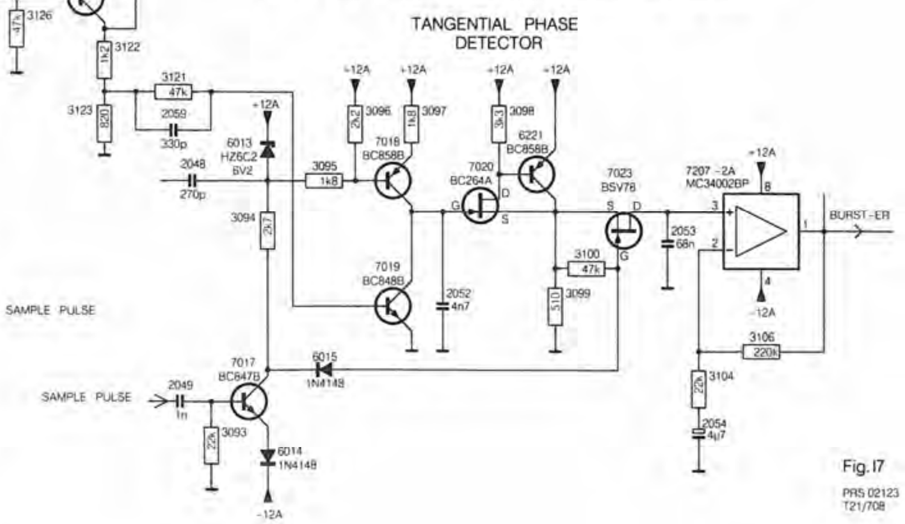


Fig.17

PRS 02123
T21/708

It is important that timebase correction is disabled during the start-up sequence until motor lock (M-LOCK) and frame lock (FRLOCK) has been reached. D6018/6019,T7024/7025 are used to clamp TANG-ER to a mean value until this moment. This mean value is realized with the aid of R3118/3119/3120 and T7026.

IC 7203 also provides the CL-VID, HMANCH and VMANCH signals. These signals are necessary for decoding the manchester codes present in the video signal from the disc. CL-VID (clipped video) is only present during a few lines in the vertical blanking. The CL-VID signal is suppressed during most of the video lines by the DO-INH signal (drop-out inhibit from the genlock module G) via T7009 and T7010.

MODULE J - FOCUS

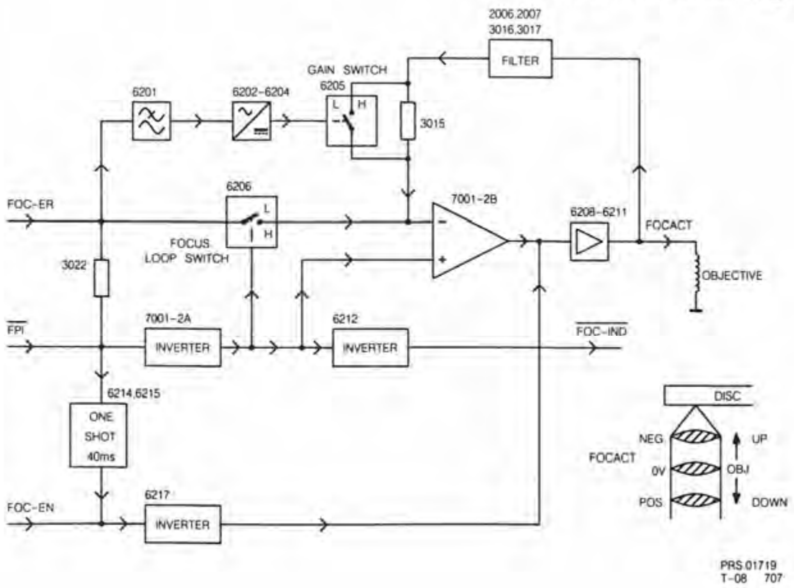
The function of the focus module is to move the objective in starting condition up to such a position that the laser beam is focussed on the disc and to keep the spot focussed under all play conditions.

Circuit description

The block diagram of the focus circuit is shown in fig.J1. The objective is driven by amplifier transistors 6208–6211, which supply a positive or negative voltage FOCACT. Negative means that the objective is driven upwards to the disc and positive means that the objective is pulled downwards. The range of the objective movement is approximately 5mm.
When the player is started up (motor not yet turning), the focus enable signal FOC-EN is low and the focus position indication signal FPI from the deck electronics is high, resulting in 0 V on the objective (see timing diagram Fig. J2). As soon as the driving module detects a disc reflection (DR), a correct slide position SPI and a laser on LA-STA the FOC-EN will go high. When FPI is still high, the drive voltage for the objective becomes negative causing the objective to go upwards. This movement is slowed down because of the feedback through filters 2006, 2007, 3015, 3016, 3017. Switch 6205 is still open, which means that there is maximum gain (low negative feedback).

When the objective focusses the laser beam onto the disc, the FPI signal will go low, causing the focus loop switch (transistor 6206) to close and after that the focus indication signal FOC-IND to go low.FOC-EN remains high. At the same time switch 6205 will be closed, which causes more negative feedback and as a consequence less gain. The FOC-IND low signal is applied to the drive module as a command that the turntable can be started. The objective is then driven by the focus error signal FOC-ER and is kept in focus by a negative voltage of average −1V on amplifier output 6208–6211.

FIG.J1 FOCUS MODULE J



When focus is found, the FPI will stay high and the drive module switches the FOC-EN to low after 0.5 sec. The drive voltage becomes 0V and the objective will move downwards. After 0.2 sec the FOC-EN will become high again and will move the objective upwards. This sequence is repeated 5 times. If no focus is found, the player is switched to stand by.

If there is a minor disturbance in the reflection, FPI and consequently also FOC-IND will become high for a short moment.
The positive pulse on FPI causes a negative drive voltage on the objective and without protection the objective should move upwards. The function of one shot transistors 6214–6215 is to prevent this. The positive FPI pulse triggers the one shot and keeps via collector of 6214 the FOC-EN signal low and via 6217/6010 the drive voltage at 0V during 40 ms. During this time the objective will not move.

The FOC-ER signal is fed through a low pass filter with transistor 6201 to an AC/DC converter with transistor 6204 and diode 6001. The DC voltage drives the gain switch in the feedback circuit of the output stage. As soon as the FOC-ER signal increases up to a certain AC level, the AC/DC converter switches the gain switch to high gain of the objective drive. The increasing error current through the objective then causes an audible noise in the LDU. When a low FOC-ER signal occurs, the circuit switches to low gain, resulting in a smooth objective drive.

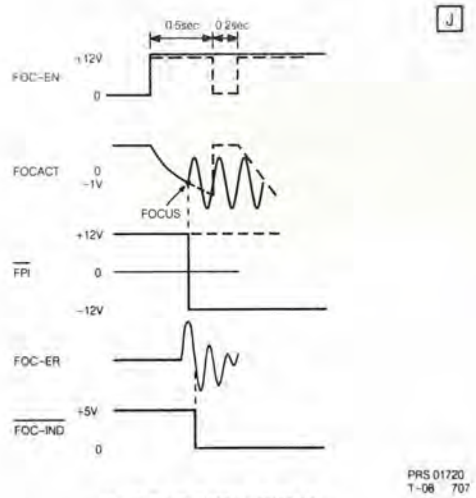


Fig.J2 TIMING DIAGRAM START UP

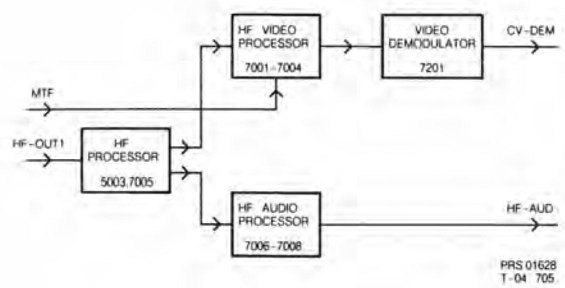
MODULE K - HF PROCESSING

The h.f. signal of the disc will be splitted up into a video and an audio signal in this module. See block diagram in Fig.K1. The h.f. signal goes to the h.f. video processor section. After a highpass filter an adaptation of the frequency response will take place there by means of the MTF voltage. This is necessary dependent on the read-out diameter of the disc. The corrected h.f. video signal will be demodulated in IC 7201. After filtering and amplification output signal CV-DEM will be available for further processing at module L (drop-out correction).
The h.f. signal also goes to the h.f. audio processor where the audio is filtered out by means of a lowpass filter. Output signal HF-AUD will be timebase corrected at module H.

Circuit description

The h.f. signal is first filtered by LC circuit 5003, 2014 and 2015. The h.f. signal will be used for the video part from the collector of transistor 7005. Therefore filtering is necessary by highpass filter (≥2 MHz) 2004, 2005, 2006 and 5001. Via amplifier stage 7002, 7003 and 7004 the h.f. video signal is available on the collector of transistor 7004. In the collector circuit of 7002 an LC circuit is situated, tuned to a frequency of 8 MHz.
The LC circuit will be damped more or less depending on the value of the MTF signal. So the MTF signal will via transistor 7001 take care of adaptation of the frequency responses.
Demodulation of the h.f. video signal takes place in IC 7201-2A with an adjustable output amplitude with the aid of potentiometer 3043. At point 16 of IC 7201-2A the demodulated video is available which will give a composite video signal (CV-DEM) after lowpass filtering (≤5MHz) and amplification by IC 7201-2B at point 6k2 of the module.
The h.f. audio signal will be obtained from the emitter of transistor 7005. This is realised with the amplifier stage in feedback mode, 7006, 7007 and 7008 and the lowpass filter (≤2MHz) in the collector circuit of transistor 7006. This filter consists of 5004 and 2019, 2020 and 2021. The h.f. audio signal is available at point 1k1 of the module.

FIG.K1 HF PROC. MODULE K



MODULE L – VIDEO DROP-OUT CORRECTION

The circuit on this module takes care of drop–out compensation of the demodulated video signal and of generation of the MTF signal. See the block diagram in Fig.L1. The drop–out detector circuit measures a negative going drop– out and in case of a drop–out it will give a pulse to switch over the DO switch to have the delayed video as output signal. This will be the case as long as there is drop–out. The drop–out pulses can be blocked by the DO–INH signal. This is necessary to prevent drop–out correction during the data part of the video signal. Drop-out correction is only done with the luminance signal. The luminance signal is fed to the CCD memory part, which takes care of the 64μs delay (one linetime).
The DC RESTORER will take care of clamping of the dc level of the delayed video to the dc level of the direct video with the aid of the burst key pulses. The MTF signal is also created on this module. This MTF signal is a dc voltage which will vary in value depending on the read–out diameter of the disc. This voltage is used to adapt the frequency response of the hf signal on the HF PROC module (K).

Circuit description

Direct video

The demodulated video signal is obtained from the HF PROC MODULE and arrives, via plug 1L1, on the base of transistor 7001. Via the emitter of 7001 the signal goes via a delay line of 470ns (5001) to the amplifier stage 7002,7003. The signal goes via emitter follower 7004 to the drop–out switch IC 7201–2A. If there is no drop–out, the video signal will, via emitter follower 7005, be available at plug 1L2.

Drop–out detection

Drop–out detection will be realised in the drop–out detector formed by IC 7202. The demodulated video goes via emitter follower 7006 to the pos.input of the opamp IC 7202, which is applied as comparator. Under normal conditions the output of the opamp is high (+12V). As soon as the pos. input will come under the switch level as a result of a drop–out, the output will become low (0V). If the video signal has no drop–out, the video level will be normal, the pos. input of the opamp will be high again. In that way a pulse is created which goes, via transistor 7007 in order to obtain the right amplitude (6V) and polarity, to pin 10 of switch IC 7201–2A.
The drop–out pulses can be blocked by the DO–INH signal. The DO–INH signal, generated on the genlock module, is present at plug 5L2. The signal is active high and will, via transistor 7008, give a low level on pin 10 of the DO switch IC 7201–2A. At that moment the switch cannot be controlled by the drop–out detector.

Delayed video

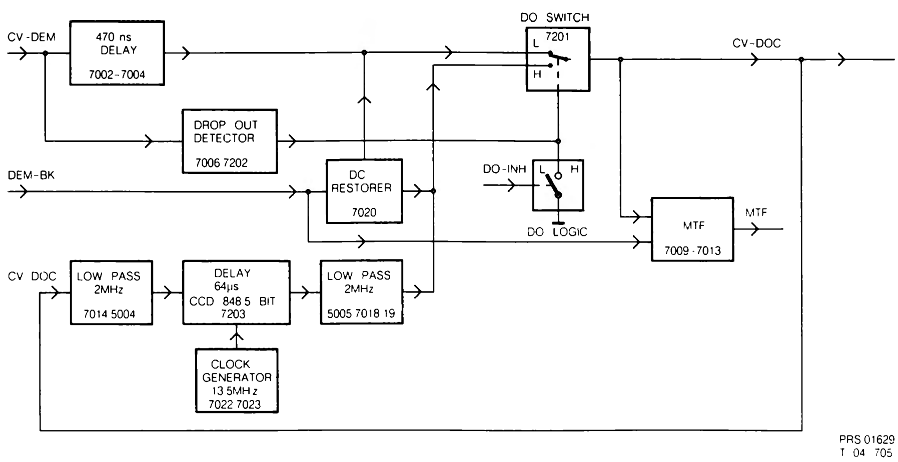
Realisation of the delayed video is done in the following way. The drop–out corrected video signal (CV–DOC) is also fed to the base of transistor 7014. In the emitter circuit a lowpass filter (≤2MHz) is provided to separate the luminance signal. The luminance signal is fed to the CCD memory IC 7203, which takes care of the 64μs delay. The output signal will be made proper again with a lowpass filter (≤2MHz) in the collector circuit of transistor 7017 and will, via transistors 7018 and 7019, be available on the emitter of transistor 7021 as video in case of a drop–out. The CCD memory needs a clock signal, which is realised with the 13.4MHz clock generator circuit (7022,7023). The frequency can be adjusted with coil 5007 to have a delay of exactly 64μs.

The DC RESTORER mainly consists of switch FET 7020 which brings the dc decoupled delayed video from the base of transistor 7021 via filter 5006 at the dc level of the direct video. This is done during the DEM–BK pulses (burst key) that are connected with the gate of FET 7020.

MTF circuit

The drop–out corrected video signal (CV–DOC) goes, via resistor 3043 and capacitor 2010 , to the base of transistor 7009. In the collector circuit of this transistor a circuit (5003/2012) which is tuned to 4.43MHz is situated.
The 4.43MHz signal will, via emitter follower 7010, go to the source of FET 7011. The gate is driven by the burstkey pulses from the genlock module (G). Transistor 7011 is only conducting during the burstkey pulses, so on the drain of this FET only the colour burst is available. The burst signal will via capacitor 2014 go to the base of transistor 7012. The burst voltage is clamped to 0.7V by the base–emittor junction of transistor 7012, so in case of a small burst the average base emittor voltage is higher than with a large burst amplitude. Consequently a large burst causes less collector current. So the collector voltage will increase and the dc–voltage across capacitor 2016 is a measure for the amplitude of the burst signal. This voltage is via transistor 7013 available at plug 6L1, it will vary between 2V and about 10V and goes to the h.f. proc module (K). This circuit is incorporated in a closed loop thus causing continuous adaptation.

FIG.L1 VIDEO DO CORR MODULE L



PRS 01629
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MODULE M - RADIAL DRIVE

The function of the radial module is, to supply the required current to drive the radial mirror in such a way that the laser beam is kept on the required track, depending on the various play modes. See the block diagram in Fig. M1.

Circuit description

In the normal play mode the radial error signal RAD–ER, originating from the deck electronics and proportional to the deviation of the laser beam relative to the track, is applied to the radial loop switch RLS transistor 7002 via a phase compensation network and a limiter IC 7100–2B. The radial loop switch, which is driven by a signal from the microprocessor 7201 on the drive processor module, is only closed when a track is followed. The radial error signal is then amplified in IC 7100–2A and via the output stage transistors 7010–7013 fed to the radial mirror. As the range of the deviation of the mirror is limited, the drive signal of the mirror is also applied via a level shifter IC 7101–2A to the drive processor. In this way too high a deviation will be compensated for by a displacement of the slide. The level shifter converts the signal, which may vary both to a positive and to a negative value, into a positive signal with the same variations.
In special play modes, the laserbeam jumps across one or more tracks. This is realised by giving the laser beam, with the aid of the radial mirror, a fast forward or reverse deviation. For this fast deviation use is made of the course pulse CP1 for a forward jump and CP2 for a reverse jump. The course pulses are also fed to the radial amplifier in IC 7100–2A. During a jump, the radial loop switch is opened by the RLS signal. The number of tracks that will be crossed in this way depends on the duration of CP1 and CP2 respectively. Both CP1 and CP2 are delivered by the drive processor module. As an indication of how many tracks are crossed, the RAD–ER signal is fed via a switchable lowpass filter in IC 7101–2B to a clipper circuit in IC 7102–2B and converted into a square wave clipped radial signal CL–RAD. The number of pulses of the CL–RAD signal, which indicates how many tracks are crossed, is fed as "count pulses" to the microprocessor on the drive processor module. In case of a jump across more than 15 tracks the radial mirror will get a high speed and about every 25 microseconds a track will be crossed. The CL–RAD signal has a frequency of about 40 kHz then with a small amplitude. In this case the switchable lowpass filter is switched to the maximum amplification of 40 kHz by the radial filter select signal RAD–FS, as a result of which sufficient signal is available again now.
During scan, a SCANLS scan loop switch "L" signal is fed to transistors 7015–7004. As a result scan loopswitch 7004 is closed and the amplification of the radial amplifier is reduced.
The TPI signal "L" on track causes switch 7003 to be closed when the beam is on track. The input voltage of the radial amplifier is present across capacitor 2014. When the beam loses track, the switch will be opened and the voltage remains on capacitor 2014. As soon as the beam is on track again, the initial input voltage for the radial amplifier is equal to the last voltage before the beam lost the track.

MODULE N - DISPLAY AND KEYBOARD

The display and keyboard module is built around a 16 bit LED driver IC 7201, driving the indication LEDs and a buzzer. See the block diagram in Fig.N1. Two control buttons are fitted : STANDBY and EJECT.

Circuit description

Input to IC 7201 takes place via the P–bus (SDAT, SCLT, DLEN) from control module S (IC 7211) as an 18 bit word, i.e. 0 + 16 data bits + terminating bit.
Outputs Q1 to Q10 are used to drive LEDs, Q11 provides an audio bleep via IC 7202 and transistor 7001.
If Q11 is "high", generator circuit IC 7202–4B, resistor 3012 and capacitor 2001 will be switched off via NAND IC 7202–4A. Pin 6 will remain "high" thus preventing transistor 7001 from starting to conduct. If Q11 is "low" and thus pin 3 of IC 7202–4A "high", IC 7202–4B will alternately give a high and a low level to output pin 6, dependent on the RC time (3012/2001).

The connections for the local switches are returned to the drive processor module (R).

FIG.N1 DISPLAY + KEYB. MODULE N

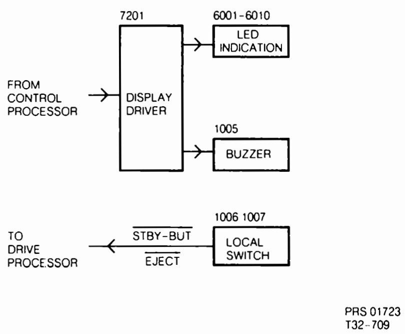
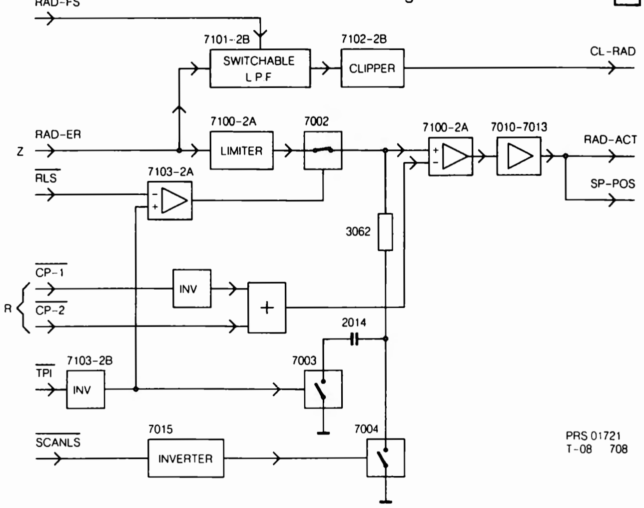


Fig.M1 RADIAL MODULE M



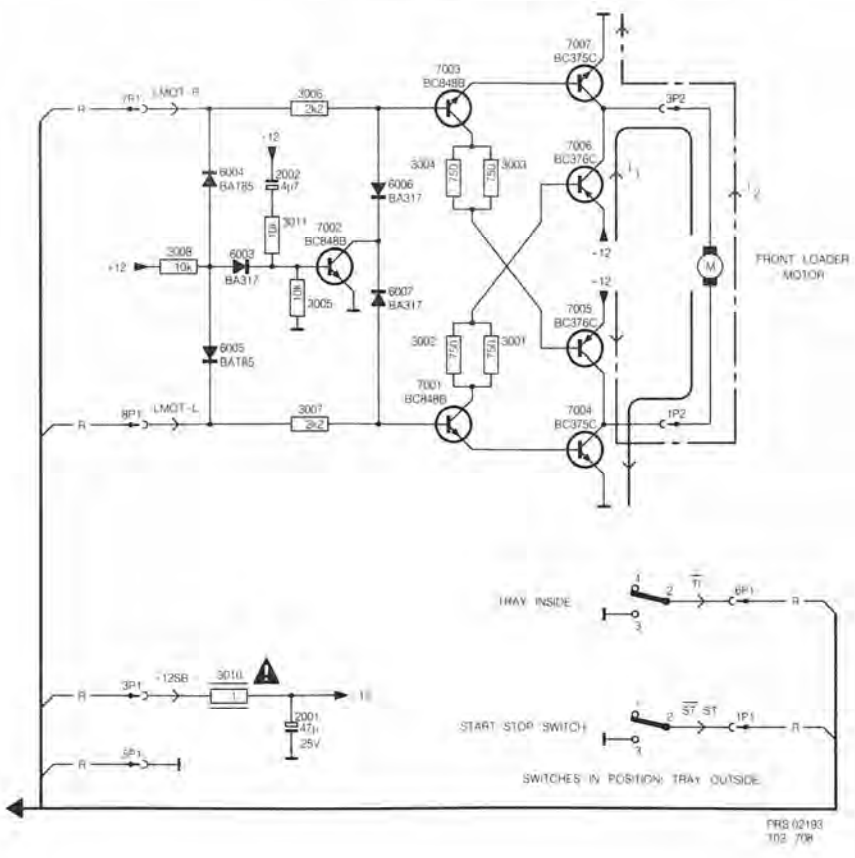
MODULE P - FRONTLOADER

The purpose of this module is to provide the required drive current to the motor of the front loading mechanism, which takes care, that the disc is positioned at the correct place in the player. Control signals are fed in from the drive processor module R and status signals are fed back to the drive processor. See Fig.P1.

Circuit description

The front loader motor is a d.c. motor, which can be driven in two ways, for loading and unloading respectively. Therefore the motor is connected to a bridge circuit. See Fig. P2.
Loading: When the tray is partly pushed in,the start stop switch is connected to ground and $\overline{\text{ST}}$-ST signal "L" is fed to drive processor R. At this moment the LMOT-L signal from drive processor R becomes "H" and transistors 7001, 7006 and 7004 will conduct. This causes current I1 to drive the motor and the tray will move further inside. When the tray is fully inside,the "tray inside" switch is closed and $\overline{\text{TI}}$ becomes "L". LMOT-L becomes "L" again and all transistors are cut off. The motor will stop.
Unloading: When "EJECT" is pressed, the drive processor delivers an LMOT-R signal "H". Now transistors 7003, 7005 and 7007 will conduct and the motor is driven by current I2. As I2 is in direction opposite to I1, the tray will now move outwards. This continues until the $\overline{\text{ST}}$-ST switch is open again and $\overline{\text{ST}}$-ST signal "H" is fed to the drive processor. LMOT-R becomes low and all transistors are blocked again.
Protection device: When the tray is blocked during loading as well as during unloading, the LMOT-L and LMOT-R signals become "L" and the motor is not energized anymore.

Fig.P1 FRONT LOADER CIRCUIT



MODULE R - DRIVE PROCESSOR

The main tasks of the drive processor module are :

- **a)** To accept and interpret commands from control module S
- **b)** Radial tracking and access
- **c)** Manchester code reading
- **d)** Display on screen drive
- **e)** Start-up sequence of the disc drive
- **f)** Local control: 'standby' and 'eject'
- **g)** Audio and video switching
- **h)** Service diagnostics

All the functions of module R run under control of microprocessor IC 7201. See the block diagram in Fig.R1. A 16k ROM is present on this module (IC 7204). The communication with control processor module S goes via the S-bus. The disc drive communication takes place via two I/O port expanders, ICs 7202 and 7203. Various drive and switching signals are given by the drive processor via the three 8-bit shift registers ICs 7213, 7214 and 7215. The drive processor reads the manchester codes of the video signal (clipped video) and also sees to insertion of the index signal.

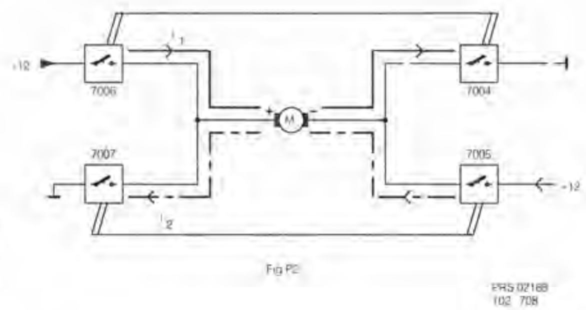


Fig P2

sub a) Command input

Command inputs from and responses to module S go via the S-bus. The S-bus interface comprises ICs 7203, 7216, 7206, 7207. IC 7203 is a port expander by which processor IC 7201 accesses S-bus handshake signals DAV and DAK.
IC 7207 is the data input buffer latch. IC 7206 is the data output buffer latch.
DAV and DAK are serviced via D-type flip flops 7216-2A and 2B.
For detailed information on the operation of the S-bus please refer to the S-bus section.

sub b) Control of the slide motor

Control of the slide motor takes place via software.
The slide motor is a stepping motor driven by the 4 phase signals COMM-1 - COMM-4 and SL-PWR which are output by port expander IC 7202.
During normal play functions the slide motor is driven when the deflection of the radial mirror is approaching its limit. This is determined by measuring the mirror offset by comparison of SP-POS (Radial error from mirror drive) with the output of DAC 7218 in IC 7210-2A. The result of this comparison (RAD-MIR) is applied to input pin 31 of port expander IC 7203.

sub c) Reading Manchester codes

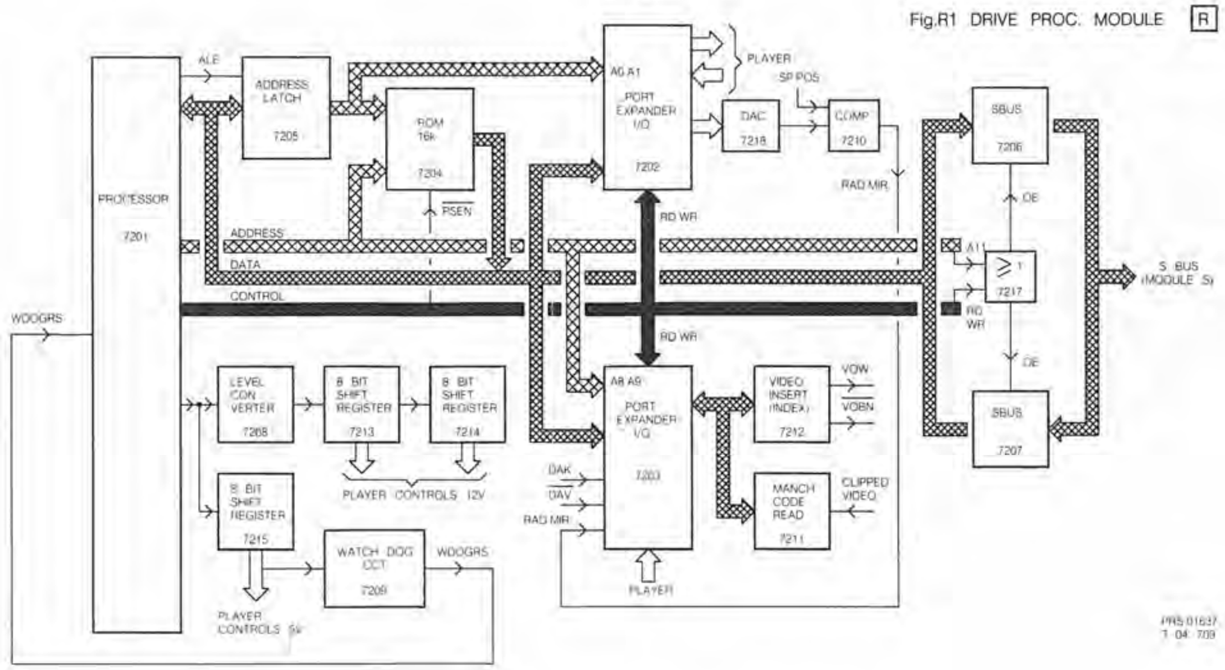
IC 7211 is a dedicated device which reads Manchester codes from the clipped video signal CL-VID. The code data is stored on-board to be read by the processor via the data bus.
Signals required by IC 7211 are :

Handshake from processor IC 7201:	$\overline{\text{ATN}}$
	$\overline{\text{TX/RX}}$
	$\overline{\text{STB}}$
	$\overline{\text{IRQ}}$
Horizontal sync	HMANCH
Vertical sync	VMANCH
Clipped video	CL-VID

sub d) Display on screen

Status information from the manchester codes for display on screen is read from IC 7211 by processor IC 7201 and loaded into display driver IC 7212.
IC 7212 contains the character generator for on screen display.

Fig.R1 DRIVE PROC. MODULE R



Inputs to IC 7212:

Databus	Pins 14-21
$\overline{\text{Reset}}$	1
$\overline{\text{HSYNC}}$	8
$\overline{\text{VSYNC}}$	7
LDI (Load index)	12

Outputs from IC 7212:

$\overline{\text{VOBN}}$ (Background for insertion)	pin 6
VOW (Character for insertion)	pin 5

To have correct timing vertical and horizontal syncs for IC 7212 are provided via IC 7219. When playing a CLV disc in the visible scan mode (internal video) the sync source is changed by NS-VID.

sub e) Start up and control

The start-up procedure has by means of a block diagram with command signals (Fig.CR1) and timing diagrams (Fig.CR2) been dealt with in chapter 2 sub 'Control routes + start-up sequence'. Here the interaction with the various modules is discussed.
The start-up sequence operates under control of processor IC 7201 via output buffers ICs 7213, 7214, 7215 and I/O port expanders 7202 and 7203. Buffers 7213 and 7214 operate with +12V supply so the input signals are first converted by level converter IC 7208. Buffer 7215 works directly with +5V supply. The start-up consists of the sequence : Close tray, move slide to start position, detect disc, activate the tilt control, put laser on, find focus, spin disc, close radial tracking loop, find picture no. 1.
During start-up it is determined which type of player we are dealing with (PAL or NTSC). This is done by determining the distance between successive VR pulses over a number of periods.
These VR pulses are the derivatives of the REFV pulses of ref. source module D. The measured period time is studied within certain limits (windows) and next the system is evaluated. If the VR signal is missing the player will not start up.

sub f) Local control

The 'stand-by' and 'eject' keys on the front of the player give, if activated, a low level signal directly to I/O port expander IC 7203. The drive processor will respond to this.

sub g) A/V switching

The drive processor sees to switching on and off of the audio and video signals, not only during start-up but also during normal play procedures. It is e.g. necessary to mute audio and video during search actions, realized with the AUD1ON, AUD2ON and CV/$\overline{\text{CS}}$ signals respectively. Or e.g. to switch over from internal source to external source if this is requested via control processor module S, realized with the A1-E/$\overline{\text{I}}$, A2-E/$\overline{\text{I}}$ and CV-E/$\overline{\text{I}}$ signals, etc.

sub h) Service diagnostics

The diagnostic software has been integrated in the drive software in such a way that many of the tasks of the drive are checked for proper performance. If a fault is detected in the execution of a task, an error code is shown on the screen as video overlay (like the index information). The software program is very useful on behalf of service diagnosis. The working and the use of this diagnosis software is dealt with extensively in the REPAIR METHOD description.

IC 7209 is a watchdog circuit which provides a reset for the processor on power up and also monitors the operation of the processor giving a reset if the program crashes.

MODULE S - CONTROL

The functions of the control module are :

a) To provide an RS232 interface between the player and an external computer.
b) To provide a local bus interface with the CPU board (UART).

Control module S is driven by processor 7201.
7201 is organised to access 64k of ROM and 64k of RAM although only 8k of RAM is fitted in the VP415/VP410.

IC 7202 is the ROM. IC 7203 is the RAM. The RAM is non volatile being supported by a 2.4V Ni-CAD battery 1002.

ROM and RAM overlay the same address field, however no conflict occurs as the control bus is fully decoded. Also the data bus pins of processor 7201 are shared with the low address byte, IC7204 functioning as an address latch under control of ALE (Address latch enable). The ROM is read enabled when PSEN (Program store enable) is low. The address bus is decoded in 3 to 8 line decoder 7205 to give 8 chip select lines (CS1 to CS8). CS1 enables RAM 7203.

The I/O ports are configured to use the top 8KBytes of memory space (E000h-FFFFh). CS8 is further decoded with A10, A11, WR, and RD to give RD1-3, RDEN, WR1, WR3 and WREN.

There are a number of I/O ports.

IC7209 - Output latch strobed by WR1 providing VP0-2. These signals are controls to the mixing board Y (via diagram Uc), in the VP415.

IC7207 - Bi-directional buffer from data bus to S-bus. Enabled by RDEN or WREN with the direction set by WREN.

IC7208 - Input buffer reading the dip switches DS1-8. Enabled by RD1.

IC7211 - A slave processor providing one RS232 I/O and two RC5 I/O's. It is addressed with A9 and WR3 or RD3 and behaves as a true slave signalling via OBF (Output buffer full) when data is ready.

IC7201 - This is the main processor which provides direct handshakes for the S-bus and a single RS232 port to service the external connector via line transmitter 7214 and line receiver 7213.

Operation

Communication with the CPU board (Module W) in the VP415 is by F-codes at 9600 baud, 1/2 duplex 5 volt logic. Communications via the external RS232 are also by F-codes but the baud rate is selectable and normal RS232 levels are used. For more information on F-codes please refer to the separate section in the operating instructions.

The default condition of module S uses the external RS232 port. The use of the internal port is selected by the CPU board module W. In this condition all F-codes presented to the external connector are ignored with the exception of mode change commands.

Memory map

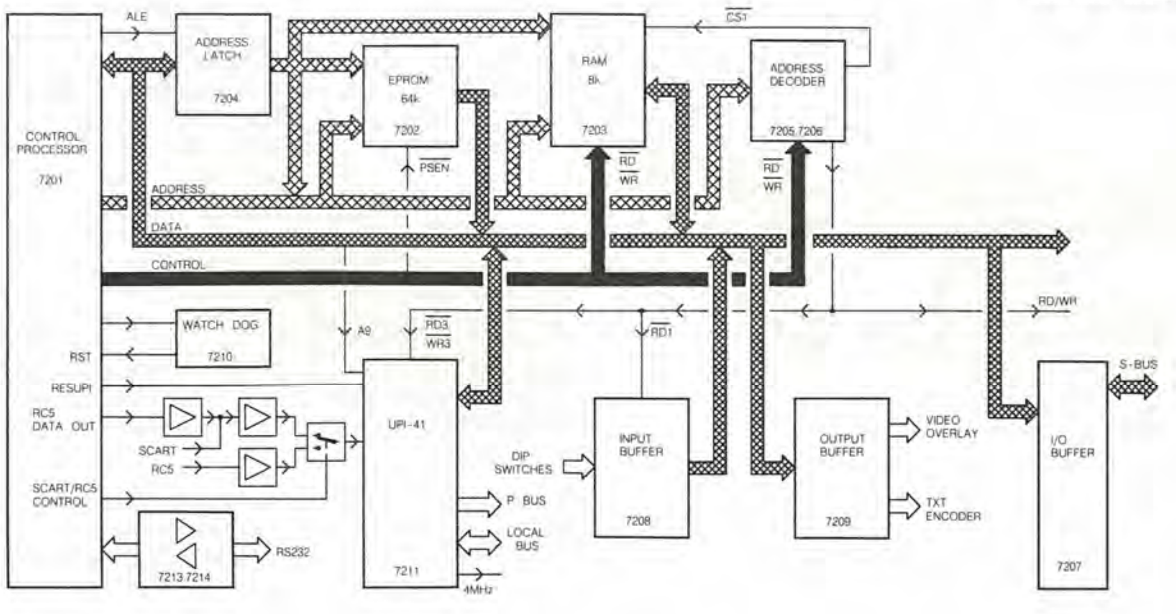
Address.

ROM (PSEN)	0000h -	FFFh
RAM (CS1)	0000h -	1FFFh
I/O ports (CS8)	E000h -	FFFFh
Address	IC.	Comment.
E000h	7207	Write to S-bus if WREN=0 else read.
E400h	7211	Slave read/write.
E600h	7211	Slave read/write.
E800h	not used.	
EC00h	7208	Read dip switches.
EC00h	7209	Write to mixer board.

Watchdog

IC7210 is a watchdog circuit which provides power on reset and also gives a reset if the program hangs up or if the local standby key is pressed. In this latter case a software reset is performed.
It consists of a retriggerable monostable which when the processor is running is continuously retriggered. At power on or if the program crashes the circuit is no longer triggered and generates a reset.

CONTROL MODULE S



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MODULE T - SUPPLY

The supply module of which the block diagram is given in Fig. T1 has as function to feed the stabilized voltages +12V, -12V, -5V and +5V to the various circuits in the disc drive. These voltages are obtained in a parallel switched mode power supply. The supply circuit is protected against overload by a current monitor. An auxiliary supply is used to generate the starting voltage for the driver stage of the switched mode power supply and the supply voltage of the command circuit.

Circuit description

The mains voltage is rectified by bridge rectifier V001. The output voltage of the bridge rectifier, which is not stabilized against mains variations, is used as supply voltage for the parallel switched mode circuit with transformer T901 and transistor V203. The switching pulses on the primary side of transformer T901 are transformed to the secondary windings 12-1, 11-2, 10-3, and x921-x922. The typical forward rectifier circuit (series and fre-wheel diode, coil and smoothing capacitor) is connected to the secondary windings and the stabilized supply voltages +12V, -12V, +5V and -5V are generated. The switching transistor V203 is controlled by the output pulses on point 5 of the command circuit D501, via a driver stage with transistor V303 and driver transformer T201. The supply voltage for the driver stage is obtained by rectifying pulses from winding 10-3 of transformer T901, by diode V301 and capacitor C301. As starting voltage for the driver stage, +15V is also generated by an auxiliary supply circuit with transistor V104 and transformer T101 (self oscillating flyback converter). This auxiliary supply voltage is also used as supply voltage for the command circuit (DS01). The command circuit generates a 50 kHz duty cycle controlled voltage, which is used as drive voltage for the driver stage. The command circuit uses the +5V input signal at pin 9 as a reference for the output voltages of the switched mode power supply. In the command circuit the voltage on pin 9 is compared with an internal reference voltage and the duty cycle of the pulses at pin 5 depends on the difference between the external voltage and the internal reference voltage. With potentiometer R503 the output voltages of the switched mode power supply can be adjusted.

Overload protection

The current in the primary of transformer T901 is proportional to the total load current. The current through transistor V203 and the primary of transformer T901 flows also through the primary of T401. This causes a voltage on the secondary side of transformer T401, across resistor R401, which is also proportional to the total load current. With the input voltage on pin 1 of command circuit D501 the duty cycle is reduced and as a consequence the output power can be limited. The level by which the current limiter starts can be adjusted by potentiometer R402. A small part of the pulses on pin 1 of D501 is applied via a voltage divider consisting of zener diode D954 and resistors R917-R916 to the base of transistor V996. During the positive pulses capacitor C506 will be discharged and the voltage on pin 12 of D501 will decrease. By this voltage level the maximum duty cycle is adjusted. This circuit is used as fast current limiter (the current limiter via pin 1 of D501 is not fast enough for transient current variations during e.g. switching on the power supply).

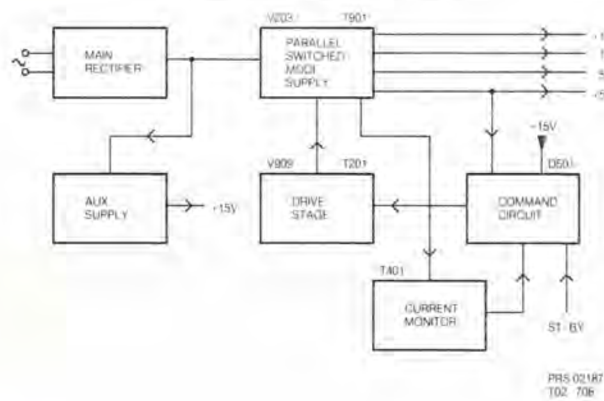
The auxiliary supply

This circuit with transistor V104 and transformer T101 consists of an oscillator and a rectifier circuit. The oscillator is of the blocking type. The current through transistor V104 is increasing until transformer T101 is saturated. From that moment on there is no voltage induced anymore in winding 1-8 and the transistor V104 will be cut off. At this moment the voltages across the windings reverse. After some time the base of transistor V104 becomes positive again and a new cycle starts. The oscillating frequency is about 30 kHz. The pulse voltage induced in secondary winding 4-5 of transformer T101 is rectified by diode V106 and capacitor C104 and forms the auxiliary supply voltage of +15V.

Output circuits

All the outputs have a common zero.
- The output +5V: winding x921-x922 of T901, rectified by series and parallel diode V701, smoothed by L701, C703. This output is also protected by fuse F913.
- The output +12V: winding 1-12 of T901, rectified by series and parallel diode V705, smoothed by L701, C707.
- The output -12V (and -5V): winding 2-11 of T901, rectified by series and parallel diode V703, smoothed by L701, C704. An additional voltage of -5V is derived from the -12V by a series regulator N801.

Fig.T1 SUPPLY MODULE T



MODULE Ua – ANALOGUE I/O CVBS + AUDIO PART

This part of module U provides selection of the various audio and video I/O configurations of the player including DC restoration of the external video input. See the block diagram in Fig.Ua1 for the CVBS circuitry and Fig.Ua2 for the audio part.

Circuit description

Sync out buffer

The comp. sync reference signal (CS–REF') will be used as sync out signal. This is realised via buffer circuit T 7109/7110 which will take care of the correct amplitude of the output signal (2Vpp) and the required output impedance. The sync out signal is available at BNC socket 6.

Sync in buffer

External sync or CVBS signals can be connected to the input BNC sockets 4 and 5. Via the buffer circuit T 7111/7112 that sync signal will be used in the disc drive as CS–EXT, which will be applied to the reference source module (D). The input is high impedance in contrast to the output. The output is made low impedance because of a wanted insensitivity to disturbances.

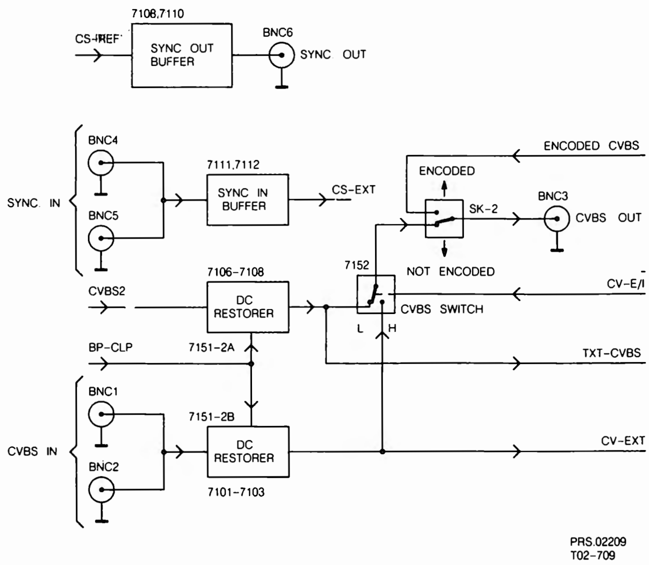
Fas–rel

A simple adjustable dc voltage (0V–8V) is used as FAS––REL signal, which will go to the ref. source module (D). This is done for adjustment of the phase relation between the incoming sync signal and the outgoing sync signal (horizontal shift). The range is from +4µs to –4µs and can be adjusted at the rear of the player.

CVBS2 via dc restorer

The CVBS signal, CVBS2, from the video processor module (C) obtains a dc restoration during the black level on the backporch of the video signal. Via the CVBS switch circuit (IC 7152) the CVBS2 is available at the BNC 3 socket, if selected. Also the CVBS2 signal is, after the DC restoration, available as TXT CVBS signal which will be fed to the TXT part of module U (Uc).
DC restoration is driven by the BP–CLP signal from the video proc. module (C). This signal goes, via buffer T 7104, to the gate of FET 7108. This FET will conduct then, so at the moment of the pulse the dc level of the CVBS signal on the collector of T 7107 will be fed to the opamp IC 7151–2A. The opamp will create an output signal which makes the dc level of the CVBS signal on the collector of T 7107 zero (pin 3 of IC 7151–2A is connected to ground).

Fig.Ua1 ANALOG I/O MODULE Ua
(CVBS PART)



CVBS IN via dc restorer

The 2 possible input sockets for CVBS IN (BNC 1 and BNC 2) are connected to each other. One of the 2 sockets can be applied as CVBS input for the disc drive itself and the other socket can be used to connect another disc drive in parallel. DC restoration takes place in exactly the same way as described in the previous section. The CVBS IN signal after DC restoration is available in the disc drive as CV–EXT signal and will be fed to the video proc. module (C) and to the CVBS switch. Then it is possible to have the external video signal directly available at the BNC3 socket depending on the control signal CV–E/$\overline{I}$ and the switch SK2.

CVBS switch

The CVBS switch is realised with IC 7152 which consists of 2 identical circuits: a switchable differential amplifier with current source. The 2 input video signals are the internal and external video signal with dc restoration. Selection of one of these signals can be done with the CV–E/$\overline{I}$ signal at plug 29cU1.
If this signal is high, the current source in IC 7152–2B will function and the CV–EXT signal will be provided to the base of T 7105 and via SK2 be available on BNC3. If the CV–E/$\overline{I}$ signal is low the switch transistor in IC 7152–2B will be cut off. In that case the circuit in IC 7152–2A will function and connect the CVBS2 signal to the base of T 7105. The signal on the emitter of T 7105 is, after division of the signal by 2, used as feedback signal to have an amplification of 2. Switch SK2 under the backplate on the rear of the disc drive can select "encoded CVBS" or "non-encoded CVBS". Non–encoded means that the video signal will not be according the standard during special playing modes.

Audio int/ext switches

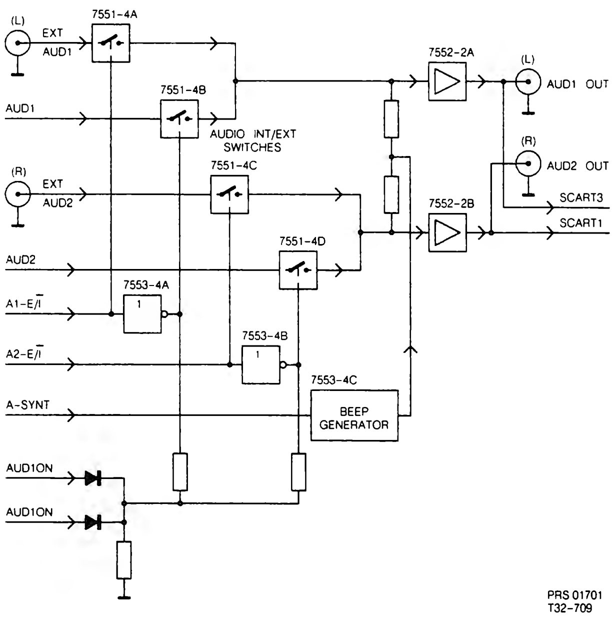
Via cinch socket "EXT AUD1" (audio left channel) the audio signal arrives at pin 11 of switch IC 7551–4A which can be driven by the A1–E/$\overline{I}$ signal at pin 12. If the A1–E/$\overline{I}$ signal is high, the switch will be closed and the external audio 1 signal will via opamp IC 7552–2A be available at the AUD-1OUT cinch bus and SCART 3 output. The A1–E/$\overline{I}$ signal closes switch IC 7551–4A if the external audio signal is asked for but will at the same time, via inverter IC 7553–4A and D 6504, open switch IC 7551–4B. So the internal AUD1 signal is switched off.
If internal audio is asked for, the A1–E/$\overline{I}$ signal will be low, so switch IC 7551–4A is open and output pin 4 of inverter IC 7553–4A is high. So this high level is blocked by D 6504 and whether switch IC 7551–4B is closed or open depends on the AUD1ON and AUD2ON signal (high level results in closed switch).
Audio switching is arranged so that if either AUD1ON = 1 or AUD2ON = 1 then both channels are active but either may be internal or external depending on the status of A1–E/$\overline{I}$ and A2E/$\overline{I}$.
For the audio 2 channel the same procedure is valid.

Beep generator

A beep generator is realised with the aid of a simple nand gate (IC 7553–4C) and can be switched on via the A–SYNT signal from the drive processor module (R). If the A–SYNT signal is low, output pin 11 of IC 7553–4C will be high and no oscillation will arise. If A–SYNT is of high level output pin 11 depends on the other input level of the nand gate (pin 13). If this level is high too, pin 11 will become low. Then C 2511 will be discharged, so pin 13 becomes low and causes output pin 11 to be high. C 2511 will be charged then via R 3528 and input pin 13 becomes high, etc. This process continues until A–SYNT becomes of a low level.
The "beep" of adjustable amplitude (R 3530) may be injected to both channels.

Fig.Ua2 ANALOG I/O MODULE Ua

(AUDIO PART)



MODULE UB – ANALOGUE I/O VIDEO PART

This part of module U re-encodes –(R–Y) and –(B–Y) as a PAL chroma signal, mixes luminance and chroma and re-inserts text from disc if it is present. New syncs are inserted then and the resulting signal output goes as CVBS to SCART and encoded CVBS to the BNC outlet socket. See the block diagram in Fig. Ub1.

Circuit description

Luminance processing

On plug 9aU1 the luminance signal LUM arrives from the RGB demodulator module (B). The LUM signal will go via an adjustable gain buffer amplifier T 7201/7202/7203 to C 2204. The luminance signal will be clamped by the BPCLP signal. This signal is available on the gate of FET 7204 and will clamp the black level of the luminance signal to about OV.

The clamped luminance signal is present on the base of T 7205. Because the base of T 7206 is at GND level T 7205 will not pass on signals of negative level. In this way the syncs are removed and the luminance signal without syncs is available on the emitters of T 7205/7206. This removing of the syncs is blocked if the NS–VID signal (plug 6cU1) is high. Because this signal can let T 7217 conduct and pull the base of T7206 to a negative voltage level. The original syncs will remain in the luminance signal. The luminance signal will be buffered by T 7207 and is then present on the base of T 7209.

The signal at the base of T 7209 will be shorted to GND if FET 7208 is conducting. This is only possible via a high level of the CBL (composite blanking) signal, which only arises in the signal parts without luminance information (line syncs, frame syncs, burst period).
This blanking is blocked again by the NS–VID signal via T 7221.

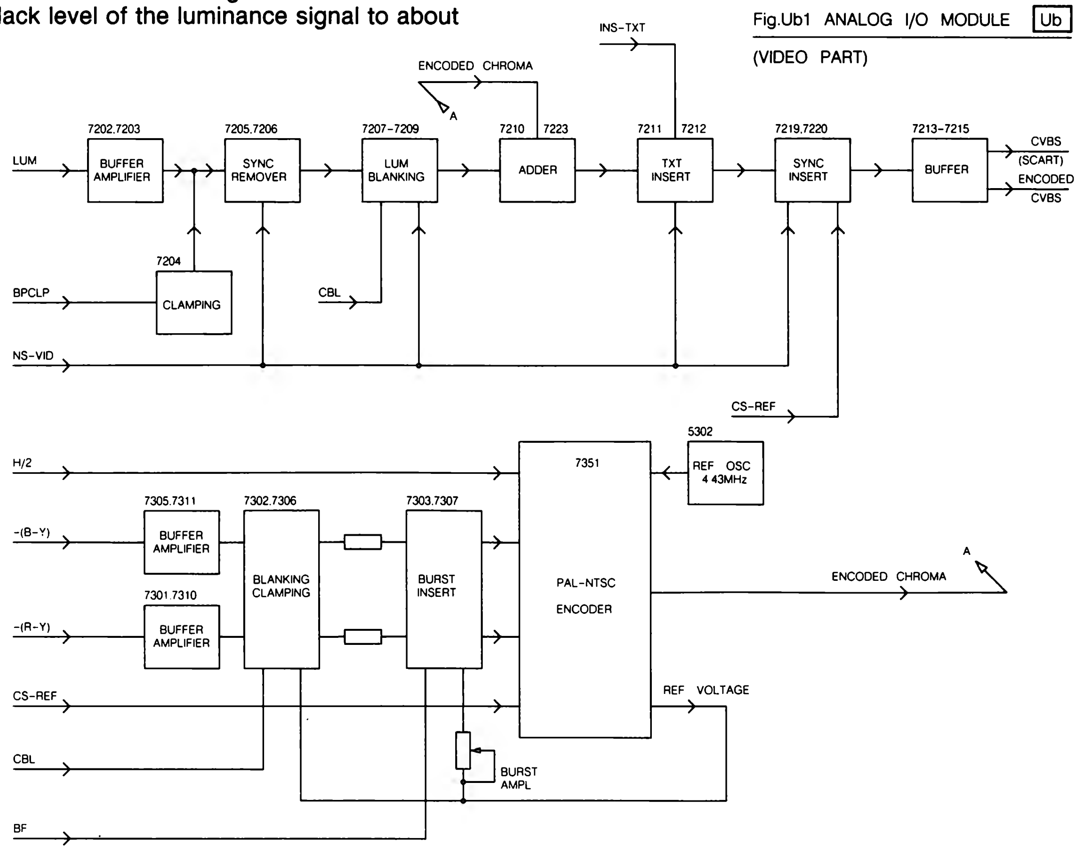
The processed luminance signal will via emitter follower T 7209 go to the base of T 7211. In the meanwhile the luminance signal will be mixed with the encoded chroma signal via L 5202. Unwanted chroma in the luminance signal will be filtered out via C 2206, L 5202 and T 7223. The encoded chroma will be added to the luminance signal via T 7210 and T 7223.

To the signal at the base of T 7211 TXT information will be added via the T 7211/7212 circuit. The amplitude of the INS–TXT signal can be adjusted by potmeter R 3240. The insertion of TXT signals can be blocked too. If wanted, the NS–VID signal will make T 7222 conducting. In that case the INS–TXT is shorted to GND, so the video signal will pass T 7211 without TXT insert. The video signal will be available at the base of T 7213.

New syncs are now added to the signal at the base of T 7213 from the CS–REF signal (generated on the REFsource module (D)), via T 7216/7219. The amplitude of the offered sync signal can be adjusted with potmeter R 3263, via T 7220. Also, the insertion of CS–REF can be blocked by the NS–VID signal via T 7218.

Fig.Ub1 ANALOG I/O MODULE Ub

(VIDEO PART)



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The complete video signal (CVBS) will go via T 7213 and the 2 emitter followers T 7214 and T 7215 to the outlet sockets SCART (pin 19) and BNC3 (CVBS out) resp.

At the moment there is non–standard video (during visible scan CLV) and the internal video is selected, the NS–VID signal (plug 6cU1, coming from the drive proc. module R) is high. If NS–VID is high the insertion of CBL, sync removing, sync insert and TXT insert will be blocked. The original luminance signal will be kept complete and is, with added chroma, directly available on the outputs.

Chroma encoding

Encoding of the chroma signal is taken care of by IC 7351. The –(B–Y) signal and the –(R–Y) signal are coming from the RGB module (B). The –(B–Y) signal is available on pin 8cU1 and will go, via inverting and buffering stage T 7305/7311 with an adjustable amplitude (R 3315), to pin 12 of IC 7351.
The –(R–Y) signal will have the same process via T 7301/7310 and is present on pin 5 of IC 7351. A crystal oscillator (5302) is connected to IC 7351 to generate the chroma subcarrier frequency of 4.43MHz.
In IC 7351 itself generation of 2 carrier signals with a relative phase difference of 90° (pin 2 and 14) takes place.
A signal with half the line frequency (H/2, from the REF SOURCE module D) is provided to pin 8 of the IC (square–wave form). This signal will take care of a 0° or 180° phase shift of the subcarrier signal to have the (R–Y) signal phase shifted 180° every second line.

Via plug 10aU1 the CBL (Composite BLanking) signal is applied to MOSFETS 7302 and 7306. These fets can be made conducting by the CBL signal, which causes the (R–Y) and (B–Y) signals to be clamped to the voltage level of pin 10 of IC 7351 offered to the sources of the MOSFETS.
This is done to prevent chroma signals during the blanking period. In that period the dc–levels on pin 12 and 5 of the IC have the same level as the reference voltage of pin 10.

Because the colour burst also has to be generated, the BF (burst flag) signal will take care of pulse creation at the right moment. The amplitude of the pulse to be added is adjustable by potmeter R 3309 for the (R–Y) signal and by R 3319 for the (B–Y) signal. The dc levels will be added to the chroma difference signals via MOSFETS 7303 and 7307. The dc level is derived from the reference voltage of pin 10 (via T 7304 and T 7308).

The signals of the (R–Y) modulator and (B–Y) modulator will be added, clamped to the reference voltage of pin 10 by the CS–REF signal on pin 7, and made available as encoded chroma signal on pin 9 of the IC. This encoded chroma signal will be inserted in the original luminance signal.

MODULE UC – ANALOGUE I/O TXT PART

In the VP415, to allow text or graphics from an external computer to be mixed with the video from the LV disc, the CVBS signal from the disc is demodulated to RGB. Text or graphics from the external source are added and the resulting signal output as RGB.
Because there is no way to pass the teletext signal from the disc by an RGB link, Module Uc provides an alternative path to the CVBS encoder. See the block diagram for the TXT bypass in Fig.Uc1.

Timing of the teletext signal is extremely important and so we find that Module Uc is built around a teletext video input processor, the so–called eye–height restorer, and a number of devices to ensure correct timing.

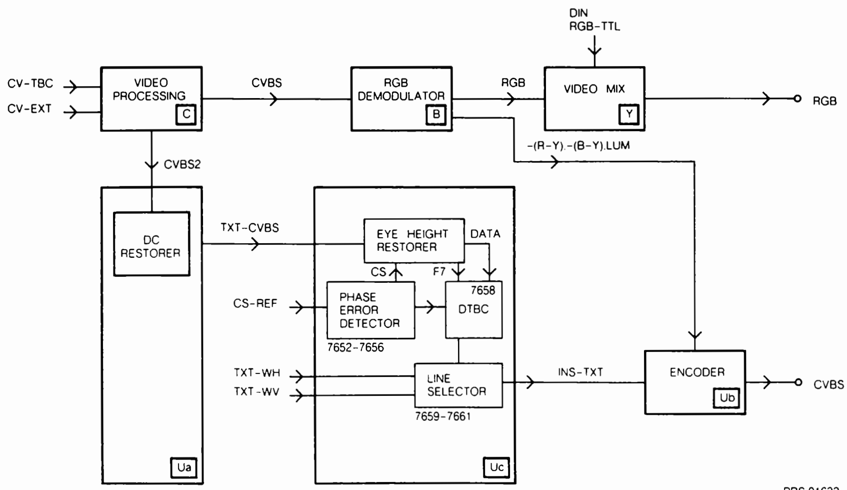
Circuit description

CVBS from the disc enters IC 7651, pin 27. In IC 7651 the text data is separated from the CVBS signal and output at pin 15. Also the bit clock (6.9375MHz) is regenerated and output at pin 14.
The text data passes via IC 7657–8C, 7658, 7661, then is inserted (INS–TXT) into the CVBS, see diagram Ub.
IC 7658 is a variable length shift register, the length (number of stages) being determined by the setting of the dip switches and the time difference between reference sync (CS–REF) and the sync signal from pin 25 of IC 7651.
The setting of the switches is pre–loaded into ICs 7655 and 7656 at the commencement of each TV line by means of CS–REF and the sync signal from pin 25 of IC 7651.

Selection of text source

In the general application of this board to the VP400 series of disc drives it is necessary to select text from CVBS or text from external (computer insertion) source as the presence of text from more than one source would confuse the decoder in the monitor.
The option of text insertion by either F–code or V–code is not available in the VP415. However, the components to allow this selection are still fitted. IC 7661 a multiplexer is present to effect this selection. Text from disc is selected when inputs 14 and 2 are both high. Input 14 is high when signal V/$\overline{C}$–TXT, plug 20cU1, is high (text from disc allowed). When input 2 is high, is determined by line counter IC 7659, 7660. Text on disc may be present during lines 20, 21, 333 and 334 of the video signal.

Fig.Uc1 SIGNAL ROUTE TXT BYPASS Uc



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MODULE W – DATA GRABBER AND CPU

Function description

We may summarise the functions of the data grabber as :-

a) Collect serial data from the LV-ROM decoder.

b) Convert the two streams of serial data to parallel form.

c) Establish lock with the block structure.

d) Read the header.

e) When the desired header is seen, store that block and the two following blocks in RAM.

f) Signal to the CPU that the header and the following three blocks are ready.

During this sequence the data is unscrambled and if error flags are present the CPU enters a correction routine to recover corrupt data.

Circuit description

The bus structure of the data grabber is as follows:

Table W1

Bus	Function
A	Address from CPU.
B	Address from byte counter.
C	Ram and eprom address.
D	Data to/from CPU.
E	Data to/from RAM.
F	Data, descrambler byte from EPROM.
G	Data, descrambled data.
H	Data from shift registers (S/P).

Bus linking

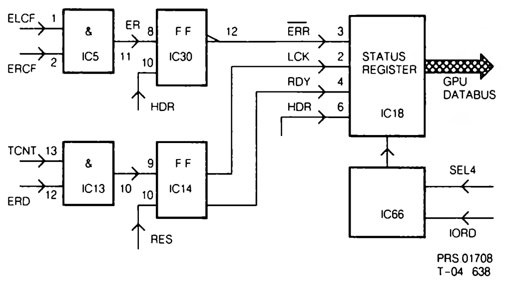
Certain of these buses can be interconnected as follows :

Table W2

Address bus C	ENW=0, to B bus	ENW=1, to A bus
Data bus E	ENW=0, to G bus	ENW=1, to D bus

Serial data from the LV-ROM decoder (DLCF,DRCF) is placed in shift registers IC9,10,11,12 to appear as 4 parallel bytes (Hbus).
These 4 bytes are strobed out under control of signals SA0-SA3
which are decoded from B0,B1 of the byte counter. Each byte from the shift registers is EXORed with a byte from the descrambler EPROM (F bus) in IC's 16,17 to appear on the G bus.
From the G bus the bytes are transferred via buffer IC21 to the RAM IC 22.
The 4 header bytes are collected in the header register IC's 19,20 the remainder of the batch of three blocks are placed in the RAM. The CPU can now read the header information to determine if this is the start of the wanted sequence of blocks.

DATA GRABBER STATUS MODULE Wa



Input circuit

Inputs from the LV-ROM decoder are via connector W1.

Table W3

DRCF	Data right	Pin 8
DLCF	Data left	Pin 4
STR1	Word strobe	Pin 5
STR2	Byte strobe	Pin 7
CLCF	Bit clock	Pin 6
ERCF	Error flag right	Pin 3
ELCF	Error flag left	Pin 2
GND	Ground	Pin 1

The incoming signals are buffered in IC's 2,3.

Sync detector

This circuit detects the sync pattern at the start of the data block. The pattern consists of a 12 byte sequence.

The detector comprises EPROM, IC 1 and D-Type flip flops IC's 6,7 and operates as a labyrinth in which, provided that the correct 96 bit pattern (8 x 12) is present an output pulse SNC will be developed. This pulse initiates the byte counter.

Sync signal SYN

This signal is used to produce a byte count in sync with the incoming data.
When SYN=1 the count is set to 000h. The count commences when SYN=0. From this point on the byte counter generates addresses for the descrambler EPROM and the RAM. Owing to the fact that SYN is produced a little early it is delayed in IC 8 to correspond with the leading edge of ST1. Error window pulse ERWD.

If ERCF or ELCF are present indicating errors uncorrected in ERCO then by ORing these signals ERWD is produced. ERWD signifies that the error correction routine must be entered by the CPU.
ERWD is stored in flip flop IC 30. IC 30 is reset by HDR when a new header is recieved.

Descrambler

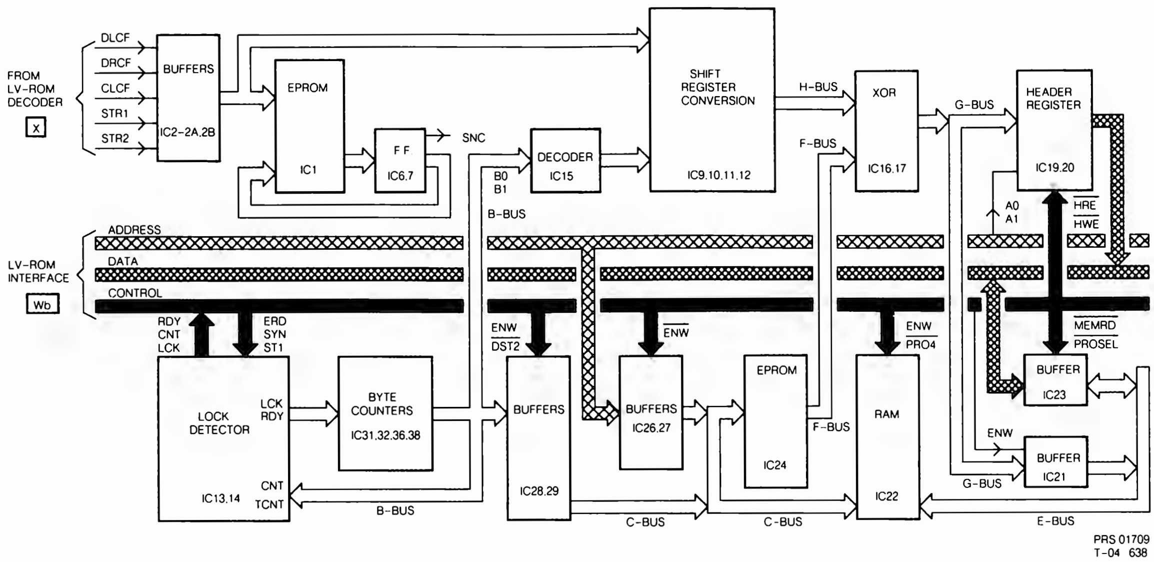
The data in each block has a superimposed scrambling pattern which must be descrambled. This is achieved by EXORing byte by byte with a descrambling pattern from EPROM IC 24. Addresses for the EPROM are given by the byte counter (C bus). The byte counter forms part of a synchronous loop which ensures that the correct descrambler byte is output by the EPROM.

In lock indication LCK

LCK indicates that the system is in lock with the block structure. LCK is derived from SYN and CNT when the byte counter is counting 2351 bytes between sync patterns (IC's 13,14).

Header pulse HDR

HDR=1 indicates that the 4 header bytes are being loaded in the header register IC 19,20 and in RAM IC 22. ERD (Enable Read Data) =1 inhibits the refreshing of the header when the header is found.



Header register

Header bytes are loaded into the header register IC's 19,20 when HWE=0 (Header write enable). Header reading by the CPU is accomplished with HRE=0, IORD=0 and SEL4=0. The CPU can then determine if the header is from the desired data block.

Byte counter

The byte counter uses 4 counters, IC's 31,32,36,38. It generates addresses for the descrambler EPROM and the RAM. The byte counter must be synchronised with the blocks. At the end of each sync pattern the counter is reset by SYN and so is rapidly pulled into lock. RDY indicates to the CPU that 3 blocks (3 x 2352) blocks are in the RAM.

RDY (ready signal)

RDY informs the CPU that 3 blocks are in the RAM. RDY is generated when TCNT(Terminate count) occurs (3 x 2352-1) from IC 35. The RDY circuit is built around IC's14,13 it is reset by RES.

Read/write of header register and RAM

The read signal comes from the CPU. The write signal is DST2=0 for the ram, HDR for the header register.

Status register

The CPU can read the status of the data grabber- port 34.

Table W4

Bit	Signal	
0	LCK	=1, Data grabber in lock
1	RDY	=1, Three blocks in RAM
2	HDR	=1, Header in register
3	ERR	=0, Error is present
4-7	Not used	

The status register is a tri-state octal buffer IC 18. It is enabled when ENA=0. ENA is derived from SEL4 and IORD in IC 66.

Processor control lines to data grabber

Table W5

-MEMRD	Read RAM
-MEMWR	Write to RAM
-IORD	Read I/O ports
-ENA	Enable status register
-PRO4	Chip select RAM 8000h - 9FFFh
-SEL4	Chip select I/O ports 40h - 4Fh

I/O ports

Table W6

-34h	Status register input
34h	Control register output
40h	Header register (Mins)
41h	Header register (Secs)
42h	Header register (Block)
43h	Header register (Mode)

RAM (8k shared with CPU)

Table W7

8000h-8003h	Header block 1
8004h-8803h	Data block 1
8804h-8923h	CRC block 1
8924h-892Fh	Sync pattern block 2
8930h-8933h	Header block 2
8934h-9133h	Data block 2
9134h-9253h	CRC block 2
9254h-925Fh	Sync pattern block 3
9260h-9263h	Header block 3
9264h-9A63h	Data block 3
9A64h-9B83h	CRC block 3
9B84h-9B8Fh	Sync block 4

Control register

Table W8

Bit	Function
1	INTR=0 Reset interupt flip flops
0 - 4	Not used
5	RES=1 Reset LCK and RDY
6	ERD=1 Read header of first data block
7	ENW=1 CPU can write to RAM

Sequence to get data from the disc

Table W9

1	Make RES=1 to reset
2	Wait for lock (LCK)
3	Wait for header
4	Make ERD=1 to read header when HDR arrives
5	Wait for ready signal (RDY)
6	Make ENW=1

CPU

The CPU section operates as the intelligent communications interface between the player and the host computer. It is built around a Z80A microprocessor and has 32k/bytes of ROM and 32k/bytes of RAM of which one 8k block is shared with the data grabber.
- Communication with the host computer is via a SCSI interface (Small Computer System Interface).
- Communication with the player is via a UART.
- Communications with the data grabber have been described.

An optional DMA controller for faster data transfer is catered for but this is not used in the VP415.

Inputs to CPU

Commands in F-Code from host computer via SCSI.
Disc data from LV-ROM decoder via data grabber.
Acknowledgements from player via UART.

Outputs of CPU

Disc dump data to host computer via SCSI.
F-Code commands to player via UART.

All three busses of the Z80A are buffered.
Address bus in IC's 44,45.
Data bus in IC 41.
Control bus in IC 40.

The RAM is arranged as 8kbyte blocks which are addressed by A0-A12. Selection of the desired block is by chip select lines -PR4 - -PR7 decoded from A13 - A15 in the 3 to 8 decoder IC56. The 3 to 8 decoder is enabled by -MREQ and gives active low outputs.

Chip enable of the ROM is by means of -PRO0 AND -PRO1 (IC 67).

In/out port arrangement

The I/O ports are arranged in 8 blocks. Each block or device is allocated a chip select signal (-SEL0 - -SEL7) which is derived from 3 to 8 line decoder IC 57 using address lines A4 to A6. The decoder is enabled when the CPU is carrying out a machine port access (IOREQ=0) and A7=0.
The block identified by SEL3 is further divided into single bit I/O ports by decoding A0 - A3 in 3 to 8 line decoder IC 58 to give -SEL30 - -SEL37. This decoder is enabled by -SEL3.

Read/write of I/O ports

When the Z80A accesses a machine port (I/O port) it does this by use of IOREQ with RD or WR. This separates I/O port access from memory access which uses MEMREQ and RD or WR.

Single bit I/O ports

The input port is built around IC 53 and consists of 8 - D-TYPE flip flops. A word is loaded from the flip flops on the rising edge of the signal derived by ORing -SEL37 and -IORD.

Table W10

Bit	Signal
0	ID0=1 interrupt from SCSI controller.
1	ID1=1 interrupt from DMA controller.
2	-
3	-
4	Baudrate=9600.
5	MON=0 Monitor enabled.
6-7	-

The output port is built around IC 53 and consists of 8 D-TYPE flip flops. A word is loaded to the flip flops from the data bus when the device is selected (-SEL34) and the write pulse (-IOWR) occurs.

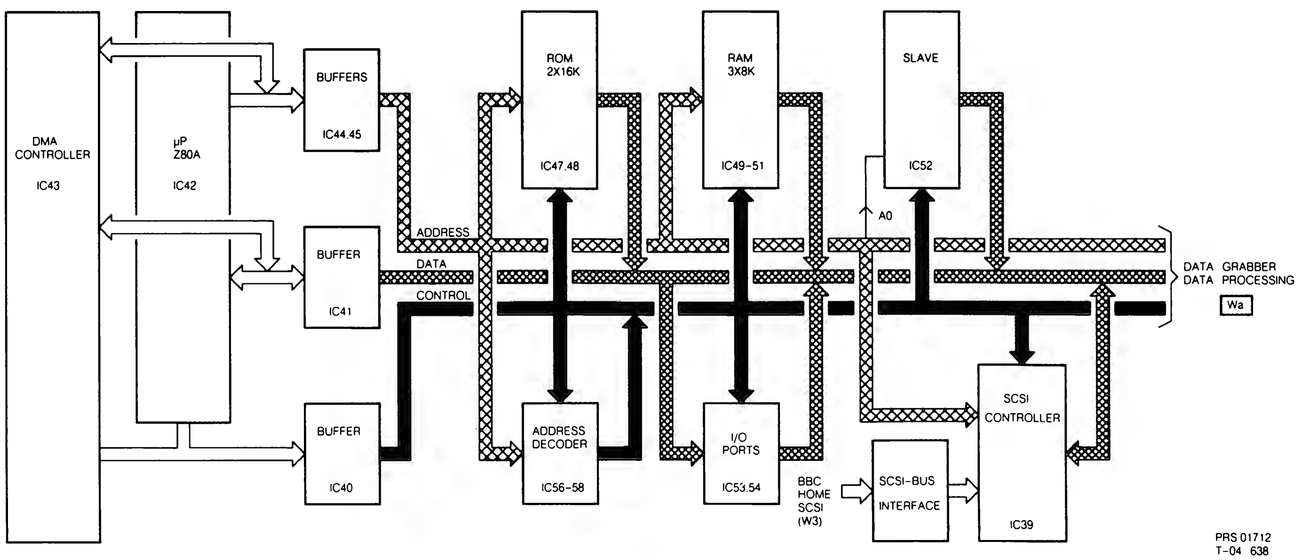
Table W11

Bit	Signal
0	INTR=0 Resets the interupt flip flops.(IC 59).
1-4	-
5	RES=1 Reset data grabber.
6	ERD=1 Enable read data.
7	ENW=1 CPU access to RAM (8000h-9FFFh).

Interrupt handling

The requirement is for two interrupt systems, one from the SCSI controller (INT0) and one from the DMA controller (-INT1). These two interrupts are combined in IC 67 and stored in J-K flip flop IC 59 to give an interrupt to the Z80A (-INT). IC 59 is reset when the interrupt has been serviced by -INTR from the output port IC 53.

LV ROM INTERFACE MODULE Wb



System clock

The 8MHz crystal clock is built around IC 63. This is divided by 2 to give a 4MHz symmetrical clock for the Z80A, DMA and SCSI and a 4MHz two phase clock for the UPI-41 .

UPI-41

The UPI-41 is a slave processor based on the 8041 providing a half duplex UART for communications with the player part.
LV-DOS (LV-ROM, Data grabber, CPU) communicates with the player via the UPI-41 RS232 interface using F-Codes.The connector for this local UART interface is W4.The UPI-41 operates via 4 internal registers, input, output, control and status. The registers are addressed by A0 with -IORD or -IORW.

Table W12

AO	-IORD	-IORW
0	output	input
1	status	control

SCSI interface (Small Computer System Interface)

All communications with the SCSI bus are under the control of the SCSI controller (NCR-5385/6).The controller has 16 on-board registers and behaves as a dedicated microprocessor.The controller can operate in target or initiator mode but for the Domesday project only target mode is used.

The SCSI registers

Table W13

port(h)	R/W	Function
00	R/W	Data
01	R/W	Command
02	R/W	Control
03	R/W	Destination ID
04	R/W	Auxilliary status
05	R	ID. register
06	R	Interrupt register
07	R	Source ID
09	R	Diagnostic status
0C	R/W	Transfer count (MSB)
0D	R/W	.. .. (2nd byte)
0E	R/W	.. .. (LSB)
0F	R/W	Reserved

There are a number of connections with the CPU circuit

Table W14

Signal	Pin	Function
	16	4MHz clock
RST	4	RST=1 resets the SCSI controller
D0-D7	1-3,43-47	Data bus to Z80A
INT0	19	Interrupt to Z80A as a result of various SCSI conditions
-IOWR	30	Active low write signal to place a byte in the SCSI
-IORD	31	Active low read pulse to read a byte from the SCSI
A0-A3	22-24,26	Addresses for the 16 registers
RDY	29	Used when a DMA controller is fitted
-SEL0	21	Chip select
-SEL30	27	Data register enable used by DMA SEL30=0 resets RDY

SCSI bus interface

Since the SCSI controller can operate in initiator as well as target mode we must consider how this selection is made.
Two control lines are used for this :-
TGS (Target group select)
IGS (Initiator group select)

The effect of these signals can be seen from the following table.

Table W15

TGS	IGS	MSG	C/D	I/O	ATN	ACK	REQ
0	0	IN	IN	IN	IN	IN	IN
0	1	IN	IN	IN	OUT	OUT	OUT
1	0	OUT	OUT	OUT	IN	IN	OUT
1	1	This is a forbidden condition					

All inputs/outputs of the SCSI bus are terminated with 220 Ohm to +5V and 330 Ohm to ground.

SCSI bus pin assignments

Table W16

Signal	Pin	Signal	Pin
-DB0	2	Ground	28
-DB1	4	Ground	30
-DB2	6	-ATN	32
-DB3	8	Ground	34
-DB4	10	-BSY	36
-DB5	12	-ACK	38
-DB6	14	-RST	40
-DB7	16	-MSG	42
-DBP	18	-SEL	44
Ground	20	-C/D	46
Ground	22	-REQ	48
Ground	24	-I/O	50
+5V	26		

In addition all odd pins numbered below 25 are connected to ground.

Indication of SCSI bus phase

.Table W17

MSG, C/D and I/O determine the bus phase

MSG	Message byte waiting
C/D	Control / Data byte
I/O	Input or output

In target mode these signals are all outputs (TGS=1). In this condition IC 71 is enabled for output and IC 70 is disabled for input.

SCSI handshake lines in target mode

Table W18

REQ informs the host computer that communications are required. ACK is the response from the host when it sees REQ. ATN informs the host that a message byte is required. BSY indicates that the device is busy.

SCSI data bus buffers

The data bus of the SCSI controller is buffered between the controller and the in/out connector. Output buffer - IC's 75,76. Input buffer IC 77. The buffers are under the control of SBEN (pin20,SCSI). SBEN=0 - output, SBEN=1 - input.

Installation of target ID

There are eight possible ID's that can be selected for the target:-
The ID is selected by means of dip switch S1 Nos 5,6 and 7.

Table W19

Dip switch setting			*ID No.*
5	6	7	
off	off	off	0 Default
off	off	on	1
off	on	off	2
off	on	on	3
on	off	off	4
on	off	on	5
on	on	off	6
on	on	on	7

CPU memory map

The CPU is organised to handle a maximum of 32kBytes of ROM plus 32kBytes of RAM.

Table W20

IC No.	*Address (h)*	*Chip select*
47 16k EPROM	0000 - 3FFF	-PRO x -PR1
48 16k EPROM	4000 - 7FFF	-PR2 x -PR3
22 8k RAM	8000 - 9FFF	-PR4 (shared)
49 8k RAM	A000 - BFFF	-PR5
50 8k RAM	C000 - DFFF	-PR6
51 8k RAM	E000 - FFFF	-PR7

CPU port map

Table W21

Port No.	*IC No.*	*Chip sel.*	*I/O*	*Function*
00	39	-SEL0	I/O	SCSI data
01	..	..	I/O	SCSI command
02	..	..	I/O	SCSI control
03	..	..	I/O	SCSI destination
04	..	..	I/O	SCSI aux.
05	..	..	In	SCSI ID.
06	..	..	In	SCSI interrupt
07	..	..	In	Source ID.
09	..	..	In	Diag. status
0C	..	..	I/O	Count MSB
0D	..	..	I/O	Count 2nd byte
0E	..	..	I/O	Count LSB
0F	..	..	I/O	Reserved - test
10	43	-SEL1	I/O	DMA data/control
20	52	-SEL2	I/O	UPI-41 data
21	52	..	In	UPI-41 status
21	52	..	Out	UPI-41 control
34	18	-SEL34	In	Data grab status
34	54	-SEL34	Out	Data grab control and interrupt reset
37	53	-SEL37	Out	Read dip sw. and interrupt f/f's.
40	19,20	-SEL4	In	Header Mins.
41	.. ..	..	In	Header Secs.
42	.. ..	..	In	Header Blocks.
43	.. ..	..	In	Header Mode.

Dip switches on the CPU panel

Dip switch S1.

Table W22

Switch	*Purpose*	
1	Baudrate selection	Not used
2	Monitor test	Not used
3-4	Not used	
5-7	Target ID installation.	

MODULE X – LV–ROM DECODER

Computer data on disc

LV-ROM data storage has a similar format to that used on the Compact Disc in that the basic word size is sixteen bits with a sample rate of 44,100 per second alternating left and right to give 176.4 kBytes/Sec.
The data is organised in blocks. Each block consists of 98 frames. Each frame contains 12 pairs of byte values (6 x DLCF, 6 x DRCF) ie. 24 bytes.
To allow syncronisation and identification each block commences with a sync pattern and header.

We can summarise a block as :

Table X1

	12 bytes sync
	4 bytes header
	2048 bytes data
	8 bytes unused
	280 bytes CRC (error detection and correction)
Total	2352 bytes

A block is read from the disc in 1/75th sec.
As the disc revolves at TV frame rate (25Hz) we may deduce that three blocks will be read during one revolution of the disc. Thus the position of any block on the disc can be obtained by dividing the block number by three to obtain the frame or picture number. The player accesses the disc in terms of frame number.

The encoding format on the disc uses a cross interleaved Reed Solomon code to give protection against reading errors caused by dust or scratches on the disc and each byte is represented by a 14 bit word. This process of modulation is termed EFM - Eight to Fourteen bit Modulation. An EFM word obeys the rule that there must be at least two and not more than ten '0's' between adjacent '1's'. Since this rule might be broken at the junction of two words three 'merging bits' are inserted between each pair of EFM words to ensure that the 2 – 10 rule is adhered to.
A 'Control and Display' word (and a syncronising pattern precede the data bytes in each frame. Two groups of parity bits each of 4 bytes complete the frame.

Over a block of 98 frames the C and D words are accumulated to provide a block label in terms of time.(Mins, Secs, 1/75 Secs)

Each frame therefore consists of

Sync pattern	24 bits
Control and display	14 bits
Data (24 x 14)	336 bits
Parity (8 x 14)	112 bits
Merging (34 x 3)	102 bits
Total bits	588 bits

In addition to the protection given by the CIRC (Cross interleaved Reed Solomon) coding further protection is provided by the 280 CRC bytes of each block.

The bit rate as read from the disc is 4.3218 Mbits/Sec. giving a decoded data rate of 153.6 kbytes/Sec.

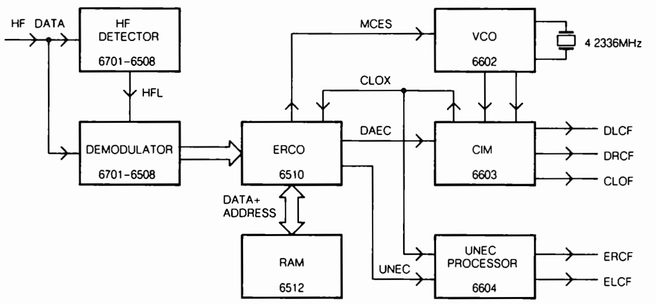
Data scrambling

There may be sections of data where a number of bytes have a similar value. This would have the effect of causing a DC offset (non-zero DSV) which could upset servo operation. To avoid this the data is modified by having a scrambling pattern superimposed. This scrambling must be unpicked in the player.

LV-ROM decoder

The LV-ROM decoder accepts the signal from module Z (HFOUT2). This signal is of sinusoidal form and carries digital data for the host computer.
The data rate is 4.3218 mbits/sec but owing to the protection overhead carried the useable data rate is 153.6 kbytes/sec.
The family of IC's used in the LV-ROM decoder is common to the Compact Disc system and so is organised to output data in 16 bit words on two channels.
Data is output in serial form as - left (DLCF) and right (DRCF) with appropriate timing signals - Bit clock (CLCF), Byte clock (STR2) and word clock (STR1). This latter references 16 bit values which are the basic units in Compact Disc.
In addition LV-ROM outputs error flags (ELCF, ERCF) to indicate if uncorrected errors remain in the data.

LV-ROM DECODER MODULE X



PRS 01630
T-04 636

Circuit description

The incoming signal from the deck is amplified (Ts6701, 6702, 6703, 6706) to give the required input level (1vpp.) then applied to the input of DEMOD (DEMODulator) IC6501. The signal is also applied to the HF level detector (Ts6530, 6531, IC6508).
When the signal is of adequate amplitude HFL, from 6508.14 enables DEMOD. This occurs when the signal is greater than 0.65Vpp.

The functions of DEMOD are as follows :

a) To regenerate a bit clock in syncronism with the bit rate from the disc.
b) To demodulate the data. (On the disc each byte is represented as a 14 bit word.)
c) To output the data with corresponding timing signals.

The bit clock is formed as a phase locked loop with varicap diode 6540 as the control element.

Signals from DEMOD are

Table X2

DADE	Data DEMOD to ERCO
FSDE	Frame sync DEMOD to ERCO
SSDE	Symbol (8 bit) sync DEMOD to ERCO
CLDE	Bit clock DEMOD to ERCO
CRI	Mutes ERCO if no data present

ERCO provides de-interleaving of the data, error detection, and error correction of up to two error bits in any word.
De-interleaving is achieved by storing the data as recieved from DEMOD in buffer RAM 6502 then picking out in the correct order.
Uncorrected errors are flagged on pin 36 of ERCO as UNEC (UNcorrected errors ERCO to CIM).
The parity bits are discarded in ERCO.

The signals from ERCO are

Table X3

DAEC	Data ERCO to CIM
UNEC	Unreliable data ERCO to CIM
CLEC	Bit clock ERCO to CIM
FSEC	Frame sync ERCO to CIM

CLOX is the master clock from CIM to ERCO which determines the rate at which data is read from RAM 6502.

CIM (Concealment, Interpolation and Muting) separates the data into left and right streams (DLCF, DRCF) and again provides the necessary timing signals STR1, STR2, CLCF (Bit clock).
There are other functions built into CIM for the Compact Disc system which are not used in this application.

UNEC descrambler

The error flags from ERCO do not correspond in time with the data leaving CIM. To restore the correct time relationship a further SAA7000 (CIM) is used, IC6604.
IC6604 provides error flags for both data streams.

Data- DLCF error flags ELCF.
Data- DRCF error flags ERCF.

Frequency of CLOX

In the Compact Disc application of this chip set the bit clock (DEMOD) runs in lock with the data from the disc which itself runs at a continually varying speed. CLOX determines the sample play rate and operates as a fixed frequency master clock. The disc is driven at a rate to maintain the contents of RAM 6512.
In this Laservision application the disc (CAV) is driven at a constant controlled speed which may be locked to an outside reference by Genlock.
ClOX therefore must run in sync with the data rate from the disc.
Provision is made to pull CLOX to the precise frequency by varicap diode 6606. The control voltage for 6606 is developed from MCES (motor control error signal from ERCO). MCES is a variable mark/space ratio signal. The mark/space ratio is determined in ERCO by the difference between the bit clock (CLDE) and CLOX. MCES is integrated by IC6602-2a and controls 6606 via 6602-2b. D6605 limits the excursions to protect 6606.

MODULE Y – VIDEO MIXING

The function of the mixer board is to allow selection of a variety of combinations of video from the disc and text/graphics from the host computer.

The combinations available are

Mode 1 Video from Laservision disc only.

Mode 2 Signals from host computer only.

Mode 3 Enhanced mode – LV 100% , 57% in window.
(In mode 3 areas of the LV video may be highlighted by windows generated by a 'black' signal from the á computer. In a window the video will be displayed at REDUCED intensity.)

Mode 4 Mix mode – 62% LV + 38% computer.
(Transparent overlay.)

Mode 5 Hard key – 100% LV or 100% computer.
(Computer text/graphics inserted in LV video.)

Mode selection is performed by control signals VP0 – 2. Video and computer signals are input as RGB drives.

Description

As the board consists of three identical channels the following description will refer only to the red channel.
The board is built around a number of TCA240 transistor arrays, each termed a mixer. To simplify the description we will allocate each array a letter.

Consider the Red channel only.

IC7151–2b	Mixer A
IC7152–2a	B
IC7152–2b	C
IC7153–2b	D
IC7153–2a	E

VP0–2 are decoded in 7458

Mode	*VP2*	*VP1*	*VP0*	*Q0*	*Q1*	*Q2*	*Q3*	*Q4*
1	0	0	0	1	0	0	0	0
2	0	0	1	0	1	0	0	0
3	0	1	0	0	0	1	0	0
4	0	1	1	0	0	0	1	0
5	1	0	0	0	0	0	0	1

The effects of the control signals on the mixers can be summarised as a table.

Mixer

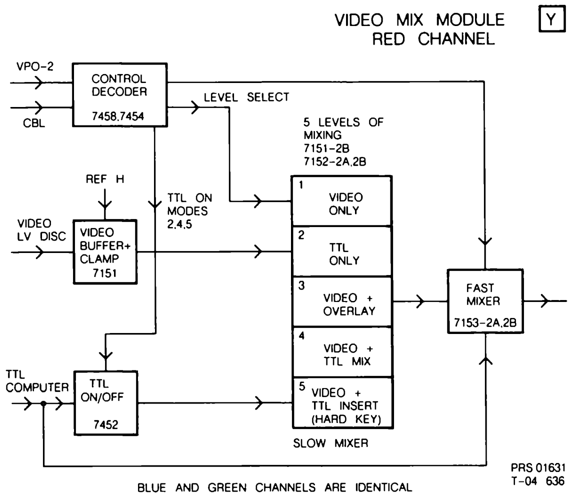
Output	*Mode*	*A*	*B*	*C*	*D*	*E*
LV–disc	1	off	off	off	off	on
Computer	2	off	off	on	on	off
Enhanced	3	on	off	off	on	on
Mix	4	off	on	off	on	on
Hard key	5	off	off	on	on	on

From this table a number of assumptions can be made

a) Mixer A passes video from the LV–disc.
b) Mixer E passes video from the LV–disc.
c) Mixers B and C pass computer video.
d) Mixer D passes computer video.

By comparing this list with the list of modes we can also deduce that mixers B and C pass differing amounts of the computer signal.

Mixer B – 38%   Mixer C – 100%.



Signal path – LV video modes 1, 3, 4 and 5

The video signal input at 9Y1 is applied to buffer/clamp 7151–2a.
During the line syncs (REFH, 1Y1) the level is clamped (7102, 7154). The signal exits 7151–2a at pin 12 to enter mixer 7151–2b pin 5. From this point the signal is also applied to mixer 71532a via R3134. The amplitude of the latter signal is determined by whether 7105 is on or off. 7105 is on in all modes except mode 3 (Reduced amplitude when 7105 is on). As mixer 7151–2b is off during modes 1, 4 and 5 the video signal will pass via 3134 and mixer 7153–2a. In mode 3 7151–2b is on to provide the signal path.

Signal path – computer video

The computer video signal input at 1Y3 is buffered and inverted by 7451–3a and applied to input 1 of 7452–3a. Output 9 of 7454–2a is high when modes 1 or 3 are selected or the burst blanking signal CBL is high causing 7452–3a to block. 74523a therefore behaves as a switch. In mode 3, RGB drives from the computer are off. A window will be generated when NOT R or G or B is sent via 7455, 7456–4a, to control input 7 of mixer 7153–2b. Due to the cross coupling between mixers 7153–2a and 7153–2b the output level of 7153–2a will be reduced.

Computer syncs

Owing to irregularities in the computer syncs these have to be restructured. Computer syncs (–CS) are applied to sync regenerator 7457 where they are regenerated and output as NS–CS (nonstandard composite syncs). When computer syncs are present the reference module (D) must be informed. The signal for this purpose is CS–S/NS. NS–CS and CS–S/NS are routed to mcdule D via module U.

MODULE Z - DECK ELECTRONICS

The Deck Electronics consist of the circuitry to process the signal from the LDU and the Active Tilt Control.
The circuits are built on a PCB, situated under the optical deck chassis. The LDU is connected to this PCB by means of a flex–foil connection. For the block diagram of the LDU signal processing see Fig.Z1.

Circuit description

The laser supply

The Solid State laser is supplied by the +5V through a controllable DC amplifier. The laser emits part of the light to the optics and part to an internal monitor–diode. This diode measures the amount of light and feeds the monitor information back to amplifier T 7005 via T 7002, 7003. In this way, a constant current through the laser is realised.
The monitor signal also drives switch T 7004, causing the LA–STA signal to go low when the laser has been switched on. This signal is fed to the drive processor module (R).
The signal LA switches, via T 7001, the controllable amplifier T 7005, thus the laser, on and off (LA low = off).

The LDU signal processing

The LDU signal processing converts the signals from the photodiodes into drive signals to be processed further in the electronics of the player.

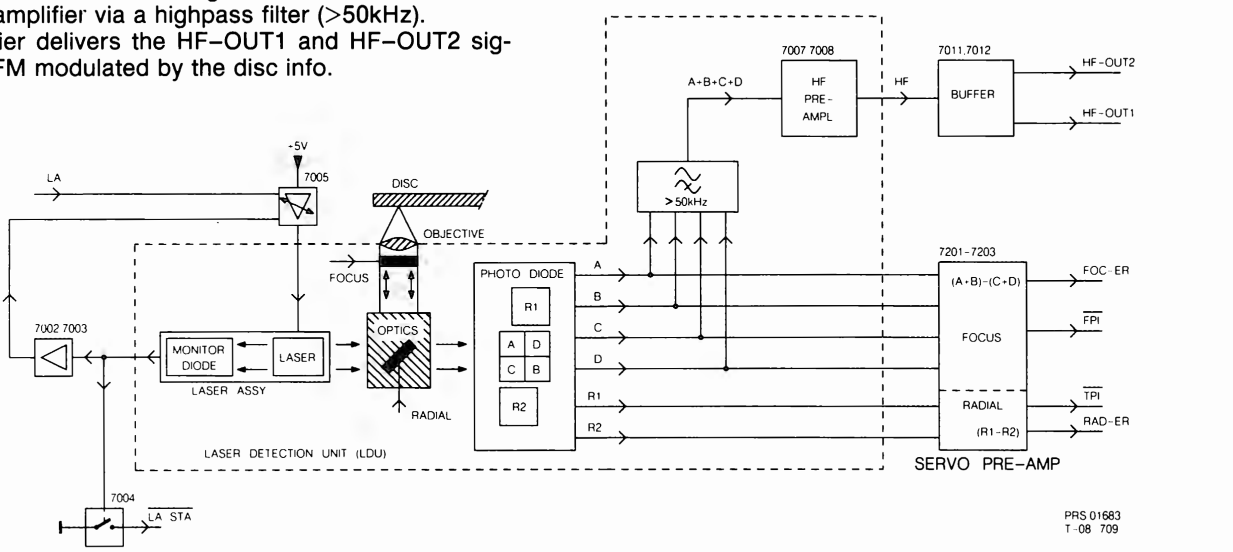
– HF signal
The signals from photodiodes A, B, C and D contain the information of the pit pattern on the video disc, read out by the laser beam. The sum signal A + B + C + D is fed to the HF preamplifier via a highpass filter (>50kHz).
This amplifier delivers the HF–OUT1 and HF–OUT2 signals, both FM modulated by the disc info.

– Radial signals
The radial fault signal on photodiodes R1 and R2 occurs when the laser spots are not exactly positioned on the tracks of the disc. In the servo preamplifier, the difference signal (R1–R2) represents the radial error signal RAD–ER. When the laser spot is exactly positioned on the track, a track position indication TPI is obtained from the servo preamp. The TPI signal is low when on track and high when the spot is off the track.
As soon as the TPI signal becomes high, the radial mirror in the LDU will be driven by the RAD–ER signal.

The ATC circuit

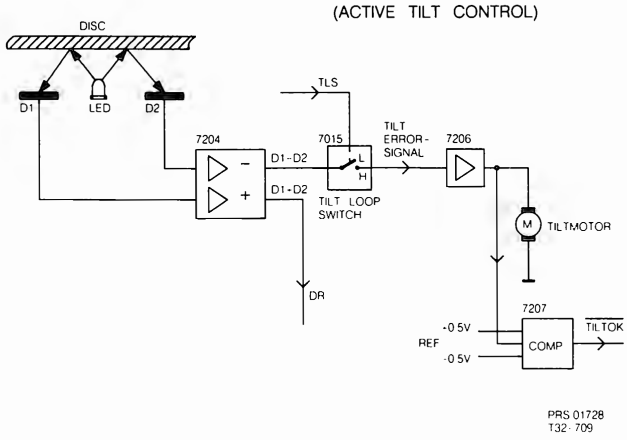
The block diagram of the ATC circuit is shown in Fig.Z2. The signals of D1 and D2 are measured in IC 7204. Addition of the two signals gives a sign that a disc is present above the LDU. In this case DR (disc reflection) is high. Subtraction of the signals represents the error–signal (D1–D2), that is fed to the tilt loop switch T 7015. Signal TLS, coming from the Drive Module, is high when the ATC circuit has to become active (DR = high).
The tilt error signal is fed to amplifier IC 7206 which drives the tilt motor. As soon as the tilt motor voltage is within a range of + and – 0.5V, the TILTOK signal will be low, as a sign that the ATC is in a correct position.

Fig.Z1 DECK ELECTRONICS (LDU SIGN. PROC.) Z



– Focus signals
The signals A, B, C and D are processed in the servo preamplifier to gain the focus error signal FOC–ER and the focus position indication FPI. Both signals drive the focus module (J) which focusses the objective onto the video disc.
The FOC–ER representing the deviation between objective and disc is composed by the difference signal (A+B) – (C+D).
The FPI signal is high when the objective is not focussed. As soon as focus is obtained, the FPI will go low and the objective is kept in focus by the FOC–ER signal.

Fig.Z2 DECK ELEKTRONICS Z
(ACTIVE TILT CONTROL)



Service Information

Chapter 8

Service Information

1987-05-18

L V Rom disc drive VP415

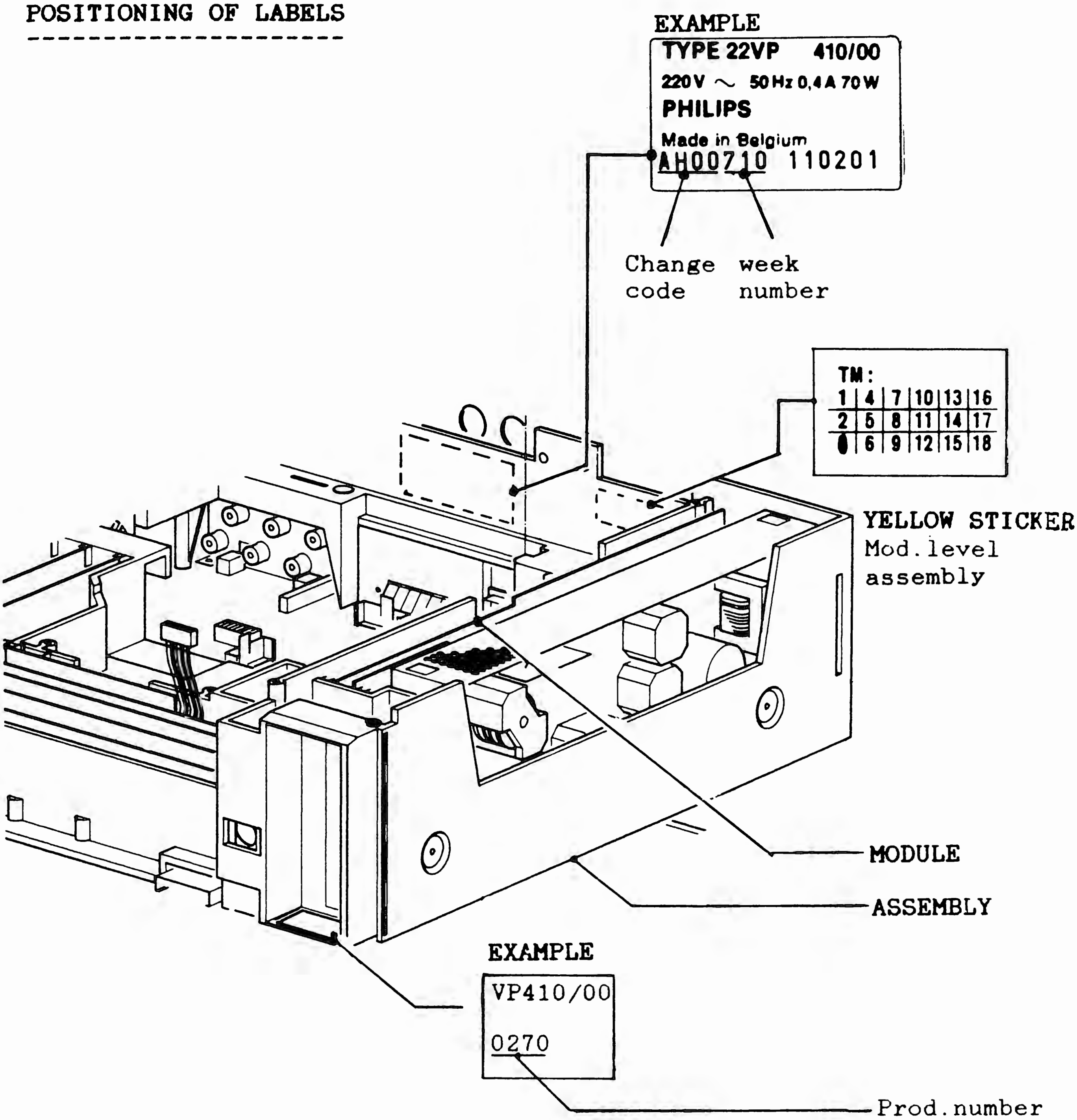
VP87-01

SURVEY OF MODIFICATIONS

CONTENTS

Service
Service
Service

POSITIONING OF LABELS



SURVEY OF MODIFICATION LEVELS VP415

- Assembly < | Change code AH.. / | Mod. level

TM :
1 4 7 10 13 16
2 5 8 11 14 17
3 6 9 12 15 18

- Modules 0 1 2 3 4 5 6 7 8 9

Week number prod. number	640-648 1 -281	649-702 281-350	703-705 351-462	706-706 463-514	707-707 515-560	707-709 561-700
-Assembly						
Change code	AH02	AH02	AH02	AH02	AH02	AH02
Mod. level	3	5	6	7	9	10
-Modules :						
A AUDIO PROCESSOR	2	2	2	2	2	3
B RGB	5	5	6	6	6	6
C VIDEO PROCESSOR	3	3	4	4	4	4
D REF SOURCE	2	2	2	2	2	2
E SLIDE DRIVE	3	3	3	3	3	3
F MOTOR SEQUENCE	5	5	5	6	6	6
G GEN LOCK	3	3	4	4	4	4
H ETBC B	5	5	5	5	5	5
I ETBC C	6	7	7	7	7	7
J FOCUS	2	2	2	2	2	2
K HF PROCESSOR	0	0	0	0	0	0
L VIDEO D.O.	0	1	1	1	1	1
M RAD	0	1	1	1	1	1
N DISPLAY KEYBOARD	1	1	1	1	1	1
P FRONT LOADER	4	4	4	4	4	4
Q RC5 MIRROR	0	0	0	0	0	0
R DRIVE PROCESSOR	3	4	5	5	5	5
S CONTROL	3	4	4	4	5	5
T SUPPLY	1	1	1	1	1	1
U ANALOG I/O	3	4	4	4	4	4
V MODULE CARRIER	1	1	1	1	1	1
W CPU DATAGR.	2	3	3	3	3	3
X LV ROM	2	2	2	2	2	2
Y VID MIX	4	5	6	6	6	6
Z DECK ELECTRONICS	2	2	2	2	3	3

Week number prod. number	710-713 701-990	713-... 991-...	...-... ...-...	...-... ...-...	...-... ...-...	...-... ...-...
-Assembly Change code Mod. level	 AH02 11	 AH03 13	 AH.. ..	 AH.. ..	 AH.. ..	 AH.. ..
-Modules :						
A AUDIO PROCESSOR	3	3	.	.	.	.
B RGB	6	7	.	.	.	.
C VIDEO PROCESSOR	4	4	.	.	.	.
D REF SOURCE	2	2	.	.	.	.
E SLIDE DRIVE	3	3	.	.	.	.
F MOTOR SEQUENCE	6	6	.	.	.	.
G GEN LOCK	4	4	.	.	.	.
H ETBC B	5	5	.	.	.	.
I ETBC C	7	7	.	.	.	.
J FOCUS	2	4	.	.	.	.
K HF PROCESSOR	0	0	.	.	.	.
L VIDEO D.O.	1	1	.	.	.	.
M RAD	2	3	.	.	.	.
N DISPLAY KEYBOARD	1	1	.	.	.	.
P FRONT LOADER	4	4	.	.	.	.
Q RC5 MIRROR	0	0	.	.	.	.
R DRIVE PROCESSOR	6	7	.	.	.	.
S CONTROL	6	8	.	.	.	.
T SUPPLY	1	1	.	.	.	.
U ANALOG I/O	4	4	.	.	.	.
V MODULE CARRIER	1	3	.	.	.	.
W CPU DATAGR.	3	3	.	.	.	.
X LV ROM	2	2	.	.	.	.
Y VID MIX	6	6	.	.	.	.
Z DECK ELECTRONICS	3	3	.	.	.	.

MOD.LEVELS PER MODULE.

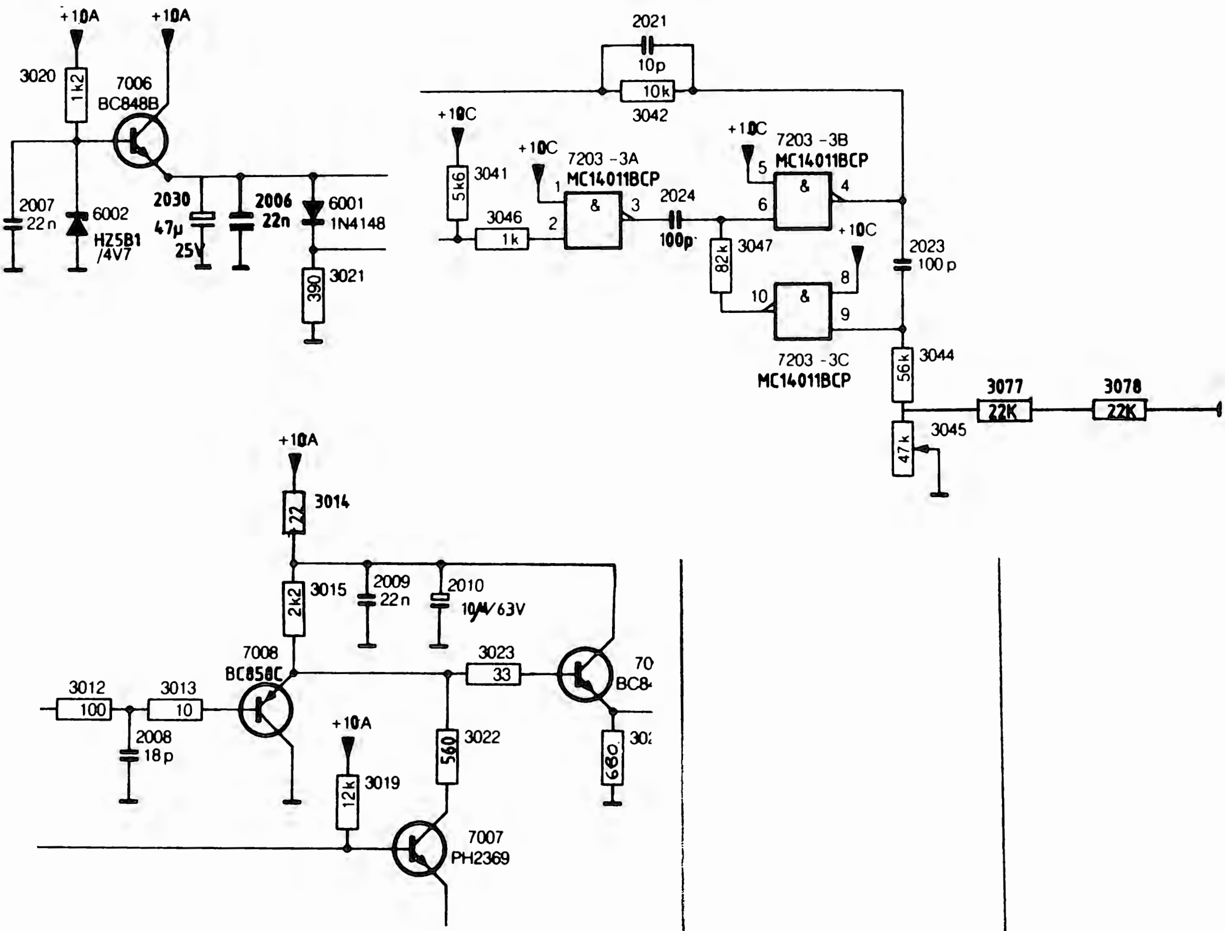
AUDIO PROC MODULE A			
Mod. level	Description	Reason	Mod. documents
3	**Deleted** : -IC6203 -R3112 47k -R3113 3k9 -R3114 2k **Added** : -TS6112 BC 817-25 4822 130 42804 -TS6113 BC 817-25 4822 130 42804 -R3075 820 E 4822 111 90171 -R3053 820 E 4822 111 90171	Availability IC,better S/R and cheaper circuit added	FA 2961

RGB MODULE B

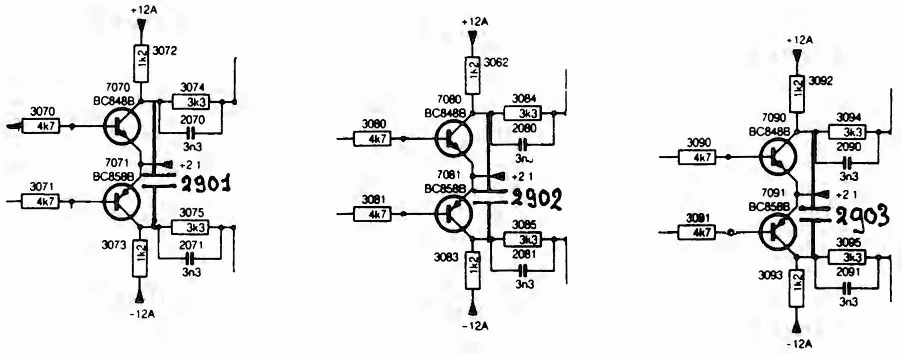
Mod. level	Description	Reason	Mod. documents
6	**Changed** : -R3031 was 3k6 becomes 3k3 4822 111 90157 -L5003 was 66μH becomes 31μH 4822 157 53155	To make the arrange level (R-Y)-(B-Y) Symmetrical	AHT 9196
7	**Changed** : -IC7202 was TDA4560 becomes TDA4565/V4 4822 209 71512 -R3021 was 10E becomes 1k 5322 111 90092 -R3022 was 1k becomes 10E 5322 111 90095 -Correction circuit diagram: .pin13-IC7202 becomes pin14 .pin24-IC7202 becomes pin13 .pin15-IC7202 to+11 supply -R3031 wasw 3k3 becomes 3k6 5322 116 53738	Improved specification	AHT9453
8	**Changed** : -Short circuit pins 27 and 28 of IC7203	White stripes at switch on and prevent neg.pulses in vert.blanking below black level	FA2989
8	**Added** : -R 22k(SFR25)between base TS7012 and 7B3(CVE/I) (Also add connection between 9C1 and 7B3 on module V)	Colour loss when 2 disc-drives operate synchronous and slave drive is in still-mode	FA2978

VIDEO PROC C

Mod. level	Description	Reason	Mod. documents
4	**Changed** : -R3007 was 130E becomes 120E 4822 111 90339 **Added** : -C2006 22N 4822 122 31797 -R3014 Fus car Flm rst 22E 4822 111 40847 -R3077 Chip rst 22K 4822 111 90251 -R3078 Chip rst 22k 4822 111 90251	Amplification extern CVBS signal is to small	AHT 9198



MOTOR + SEQUENCE MODULE F

Mod. level	Description	Reason	Mod. documents
6	**Deleted** : -C2010/2011/2012/2013/2014 2015 **Added** : -C2901/2902/2903-1n2 4822 122 10185	White dots on screen	FA2960 FA2968
			
6	**Changed** : -C2020 was 4µF becomes 1µF 4822 124 22028	Improved lock in of 6"-and 8"- disc	FA2976
6	**Changed** : -C2002 was chip 330nF becomes Pol.cond. 330nF 4822 121 42779 -R3015 was 1k5 becomes MET FLM RST 1k5	Unallowed tol-erance and instability of motor control-loop.	FA2981
6	**Changed** : -IC7260 was MC1458P1 becomes MC34002BP 4822 209 71382	Improved GOTO at CLV	AHT9921

GEN.LOCK **G**

Mod. level	Description	Reason	Mod. documents
4	**Changed** : -R3077 was 100k becomes 91k 5322 111 90277	Shift of DO-INH window	FA2955

ETBC B MODULE H

Mod. level	Description	Reason	Mod. documents
5	**Changed** : -R3072 was 3K4 becomes 2K4 4822 111 90286 -2070 was 47PF becomes 39PF 4822 122 31069	Fault in diagram	FA2894 AHT9064 AHT8790
5	**Changed** : -R3013 was 22k potmeter, becomes 2k2 potmeter 5322 101 14008	Improved adjustment of VCO at CLV disc	FA2947 AHT9095
5	**Deleted** : -C2059/2061/2064 -R3115/3116/3120/3121/3122 3123/3124/3125 -L5009/5010/5011 -D6013 -TS7026/7029 **Changed** : -R3127 was 620E becomes 22k 4822 111 90251 -R3130 was 470E becomes 1k 5322 111 90092	Audio correction is not necessary	AHT9069
5	**Changed** : -C2001 was 270nF becomes 220nF 4822 121 41876	Fault in diagram	AHT9349

ETBC-C MODULE I

Mod. level	Description	Reason	Mod. documents
7	**Changed** : -C2046 was 56PF becomes 47PF 4822 122 31772	Decrease of disturbation on time fault measuring	AHT9061 FA2945
7	**Changed** : -C2015 was Pol 100nF becomes Cr chip 100nF 5322 122 32839 -C2023 was Pol 33nF becomes Cr chip 33nF 5322 122 31848 -C2024 was Pol 270nF becomes Cr chip 270nF 5322 122 32839	Improvement of HF filtering in sync separator	AHT9348

FOCUS MODULE J

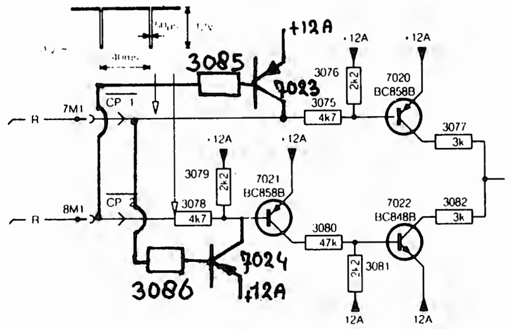
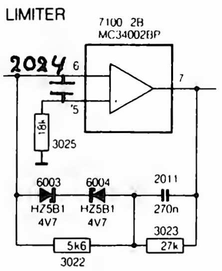
Mod. level	Description	Reason	Mod. documents
3	**Changed** : -R3025 was 4k7 becomes 2k7 4822 111 90569	Improvement of playability	FA2974
4	**Added** : -R3055 10k SFR25 on connector 7J1 to mass 4822 116 52973	Prevent FOC-EN to go active when drive is in "tri-state"	FA2988

HF PROC MODULE K			
Mod. level	Description	Reason	Mod. documents
1	**Changed** : -R3015 was 470E becomes 120E 4822 111 90339	Avoid limiting of HF ampli- fier at max. resonant rise	AHT9286

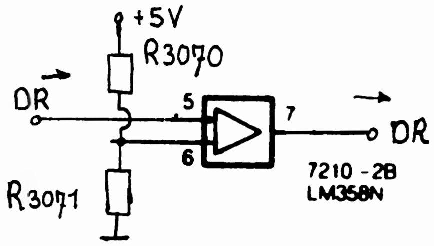
VIDEO CORR MODULE L

Mod. level	Description	Reason	Mod. documents
1	**Changed** : -R3096 was 470E becomes 560E 5322 111 90113	Adaption of video amplitudes	AHT9062
1	**Changed** : -R3046 was 3k3 becomes 2k7 4822 111 90157	MTF-regulation is not good	AHT9287

RADIAL MODULE M

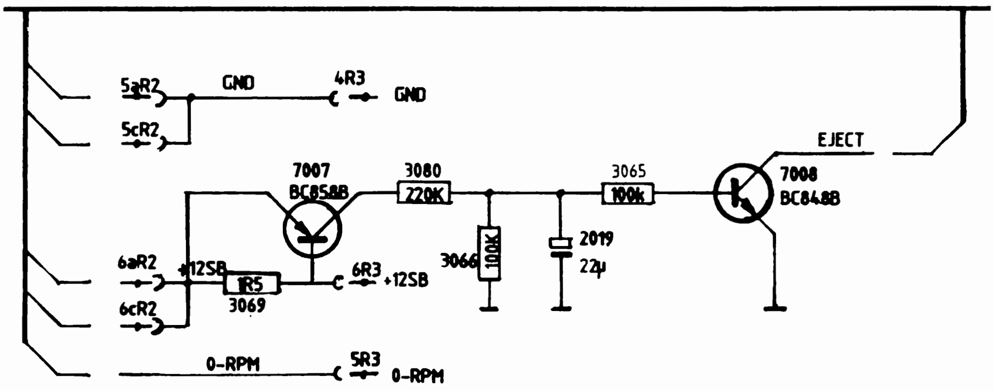
Mod. level	Description	Reason	Mod. documents
1	**Added** : -TS7023 BC558B 4822 130 44197 -TS7024 BC558B 4822 130 44197 -R3085 47K 4822 116 52472 -R3086 47K 4822 116 52472 	Avoid DC offset on radial mirror unload	FA2946
2	**Deleted** : -TS7023 BC558B -TS7024 BC558B -R3085 47K -R3086 47K	New drive software 6803.5 on Drive Proc. Mod.R	FA2946
2	**Deleted** : -R3001/3002/3003/3004/3005 -R3006/3007/3008/3009/3010 -C2002/2004 -TS7001-Short circuit S en D of TS7001	Improvement jump behaviour	AHT9350
2	**Deleted** : -TS7004	Idem	FA2958
3	**Added** : -C2024 10pF 4822 122 32185 	Avoid oscil-lation on TS IC7100	FA2983

DRIVE PROC MODULE R

Mod. level	Description	Reason	Mod. documents
-	**Changed** : -R3064 becomes R3069 -R3064 becomes R3080 -C2019 was 10µF becomes 22µF 5322 124 21643	Correction Service manual	AHT9285
4	**Changed** : -EPROM IC7204 software was 3104 103 6803.4 becomes 3104 103 6803.5	See survey of software rel-eases in this service infor-mation	WV14748
5	**Added** : -R3070 100k 4822 116 52453 -R3071 100k 4822 116 52453 	Improvement of DR-signal	AHT9285
5	**Changed** : -C2004 was 2µF becomes 10µF 5322 124 21749	A temporary solution to avoid "reset" of the drive	FA2889 AHT9457
6	**Changed** : -EPROM IC7204 software was 3104 103 6803.5 becomes 3104 103 6803.6	See survey of S.W releases in this Ser-vice Informat-ion	WV14750
7	**Changed** : -C2018 was 15µF becomes 68µF 5322 124 10512	Prevent eject of disc tray at start up	FA2990

DRIVE PROC MODULE R(CONT'D)

Mod. level	Description	Reason	Mod. documents
7	**Added** : -R3064 1E5 4822 111 30487 -R3065 220k 4822 111 90197 -R3066 100k 4822 111 90214 -R3067 100k 4822 111 90214 -C2019 10µF 5322 124 21749 -TS7007 BC858B 5322 130 41983 -TS7008 BC848B 5322 130 41982	Finger protection circuit front loader	AHT9030



CONTROL MODULE S

Mod. level	Description	Reason	Mod. documents
-	**Changed** : -R3005 was 10K becomes 8K2 5322 111 90118 -R3006 was 47K becomes 10K 4822 111 40249 -R3012 was 10K becomes 2K7 4822 111 90569	Correction of Service manual	
6	**Changed** : -EPROM IC7202 software was 3104 103 6804.4 becomes 3104 103 6804.5	See survey of S.W releases in this Service information	WV14748
7	**Changed** : -EPROM IC7202 software was 3104 103 6804.5 becomes 3104 103 6804.6	See survey of S.W releases in this Service information	WV14749

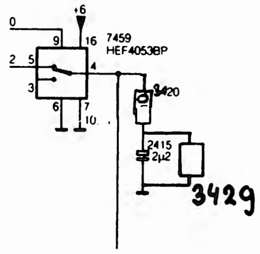
SUPPLY MODULE T

Mod. level	Description	Reason	Mod. documents
1	**Added** : -Res. 0.15E/1W 5322 113 41136 in series with fuse F913. Only for VP410.	Stripes in picture at start up of disc drive	FA2954

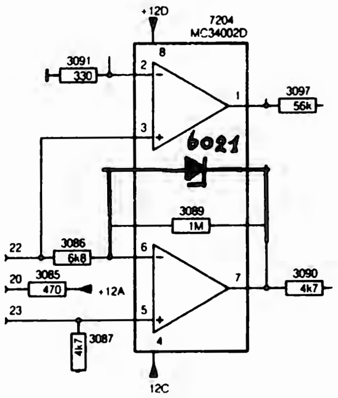
ANALOG I/O MODULE U

Mod. level	Description	Reason	Mod. documents
4	**Changed** : -R3304 was 470E becomes 330E 5322 111 90106	Arrange level too small	FA2934 AH18876
4	**Added** : -R3350 100E in series with C2302 5322 111 90091 -R3351 100E in series with C2305 5322 111 90091	Improvement CBL to encoder Analog I/O	FA2948
4	**Changed** : -IC7651 was IC SAA5230/V3 becomes IC SAA5231/V3 4822 209 71491	Availability of IC	AHT9548

VIDEO MIX MODULE Y

Mod. level	Description	Reason	Mod. documents
5	**Changed** : -D6404 was BB112 becomes BB809 5322 130 31684	Correction Ser.manual	AHT9032 FA2908
5	**Changed** : -C2416 was 8nF2 becomes 100pF 4822 122 32942	Improvement horizontal distortion computer text	FA2943 AHT9352
6	**Added** : -R3429 Chip rest 10M 4822 111 90807 	Jitter of com- puter overlay	FA2949 AHT9197

DECK ELECTRONICS Z

Mod. level	Description	Reason	Mod. documents
-	**Changed** : -R3104 was 22K becomes 10K 4822 111 90249 -R3086 was 6K8 becomes 33K 5322 111 90267 -R3087 was 4K7 becomes 22K 4822 111 90251 -R3088 was 4K7 becomes 22K 4822 100 11155 -R3089 was 1M becomes 4M7 4822 111 90806	Fault in diagram Introducing new corner sensor with another specification	FA2950
-	**Added** : -D6021 HZA92 8V2 4822 130 33294 **Changed** : -R3109 was 10E becomes 0E 4822 111 90163 -R3110 was 10E becomes 0E 4822 111 90163 	Tiltmotor does not work correct	FA2880 AHT9134
-	**Changed** : -D6021 was HZA92 becomes BC548B 4822 130 40937.	Cheaper	AHT9863

SURVEY OF SOFTWARE RELEASES VP410/415.

MODULE	ITEM	NAME	PROGR NBR 3104 103	SW REV LEVEL	INTRODUCTION. DATE	CHECKSUM	SERVICE CODE NBR 4822 209 .....
DRIVE PROC(R)	7204	DRIVE	6803.4	1.5	1986-10-30	B5F1	51257
			6803.5	1.6	1986-11-24	9DB6	51257
			6803.6	1.7	1987-02-23	68FF	51257
CONTROL (S)	7202	CONTROL	6804.4	1.4	1986-10-30	1F53	51256
			6804.5	1.5	1986-11-24	2B55	51256
			6804.6	1.6	1987-02-09	5D44	51256
			6804.7	1.7	1987-02-23	C699	51256
			6804.9	1.8	1987-03-19	6728	51256
*CPU (W)	7201	SYNC	6808.0	1.0	1986-10-30	D120	51258
*CPU (W)	7224	DESCR.	6807.0	1.0	1986-10-30	1FBE	51259
*CPU (W)	7247	LVDOS#1	6805.2	1.3	1986-10-30	B42D	** 51261
			6805.3	1.4	1986-11-24	BF90	** 51261
*CPU (W)	7248	LVDOS#2	6806.2	1.3	1986-10-30	1A1C	** 51262
			6806.3	1.4	1986-11-24	56D7	** 51262

ATTENTION!

*ONLY VP415

**ORDER BOTH SERVICE CODENUMBERS OF LV DOS WHEN THE PROGRAMNUMBER OF THE EPROM'S IN THE SET TO BE REPAIRED DEVIATES FROM THE LATEST PROGRAMNUMBER

Survey of software releases VP410/415

Description of software modifications

DRIVE (on mod.R)

Progr. No. 3104 103	changed with respect to earlier release	Ref.doc AR33	SW Rev level
6803.4	First release.	--	1.5
6803.5	-Eject of disc tray when no disc has been inserted -Delayed closing of radial mirror loop at start up of motor. -Improved SCAN FRWD action. -Improved jump behaviour. -Adaptation of STAND-BY command.	2125-087	1.6
6803.6	-Improved catch-in behaviour instant jump. -Influence of phase of 2-PPR signal deleted. -Adaptation of 2-PPR signal. -Measurement of radial mirror sensitivity adapted -Error code report commutation added (codes 77 & 78).	2125-100	1.7

CONTROL(on mod.S)

Progr. no. 3104 103	changed with respect to earlier release	Ref.doc AR33	SW Rev level
6804.4	First release.	-	1.4
6804.5	-Several problems on S-bus, RC-5 and F-code communication solved.	2125-089	1.5
6804.6	-Improved goto time and chapter CLV. -Improved chapter play CAV -Prevent"stand by"when drive is in "replay"mode.	2125-098	1.6
6804.7	-Correction on"stand by" problem described under rel.1.6. -Improved character display in programming mode.	2125-106	1.7
6804.8	-Not produced.		-
6804.9	-Switching the interval in the S-bus task when the eject button is pressed in the"ready"-mode of the drive.This avoids the switching to"stand by" after elapse of the interval time(75 sec). -Changed acknowledge handling of the F-code interpreter -Improved chapter play when drive is in replay. -Repeat LED off when drive is in the"ready"-mode.	2125-116	1.8

SYNC (on mod.W)

Progr. no. 3104 103	changed with respect to earlier release	Ref.doc	SW Rev level
6808.0	-First release.	-	1.0

DESCRAMBLER (on mod.W)

Progr. no. 3104 103	changed with respect to earlier release	Ref.doc	SW Rev level
6807.0	-First release.	-	1.0

LV-DOS# 1 + LV-DOS# 2 (on mod.W)

Progr. no. 3104 103	changed with respect to earlier release	Ref.doc AR33	SW Rev level
6805.2 + 6806.2	-First release.	-	1.3
6805.3 + 6806.3	-Prevent hang-up of drive at internal communication between LV-DOS and CONTROL -"Reset to default command" replaced by setting the defaults with separate F-code commands.	2125-088	1.4

IMPORTANT:

When ordering a service codenumber for LV-DOS EPROM, the program number in the set should be checked.
The delivered EPROM is always equipped with the latest software release. If your set to be repaired is equipped with a lower release level, both LV-DOS# 1 and LV-DOS# 2 should be ordered and replaced.

FAULT SYMPTOMS AND SOLUTIONS

This survey describes a number of known fault symptoms or problems,that can occur in the disc drive.
A possible solution for mentioned problems is given and also is indicated when the solution has been introduced.

The problems have been divided into several categories, each with an increasing following order number.
Undermentioned categories have been choosen :

A = START UP PROBLEMS
B = PLAYABILITY PROBLEMS
C = AUDIO PROBLEMS
D = VIDEO PROBLEMS
E = COMMUNICATION PROBLEMS

START UP PROBLEMS

Number : A 1

Problem : Disc tray opens when starting up.

Solution : Change C2018 on Drive Proc.module R from 15 μF into 68 μF.

Introduced : Module R : mod level 7

Number : A 2

Problem : No eject of disc tray when no disc has been inserted.

Solution : Update in Drive software on Drive Proc. module R (6803.5)

Introduced : Module R : mod. level 4.

Number : A 3

Problem : Start up problem when loading 6" or 8" disc.

Solution : Change C2020 from 4μF into 1μF on MOTOR module F.

Introduced : Module F : mod. level 6.

Number : A 4

Problem : White stripes on screen when disc drive is switched on.

Solution : Short circuit pins 27 and 28 of IC 7203 on RGB module B.

Introduced : Module B : mod level 8

Number : A 5

Problem : Horizontal stripes in picture at start up of disc drive (only for VP410)

Solution : Add resistor 0,15E/1W in series with fuse F913 on supply module T.

Introduced : Module T : mod level 1

PLAYABILITY PROBLEMS

Number : B 1

Problem : Instant jump failures

Solution : -Delete R3001 upto R3010,C2002,C2004,TS7001 and TS7004 on Radial module M.

-Several updates in Drive software on Drive Proc. module R (6803.5 and .6

Introduced : Module M : mod. level 2
Module R : mod. level 4 and 6

Number : B 2

Problem : Goto failures at CLV.

Solution : Change IC7260 on MOTOR + SEQ module F from MC1458P1 into MC34002BP.

Introduced : Module F : mod level 6

VIDEO PROBLEMS

Number : D 1

Problem : White dots on monitor screen
(motor disturbance in video signal)

Solution : Mount metal screening around coils L5001 and L5002 on HF PROC module K and metal screening around delay line L5001 on VIDEO DO CORR module L. Screening assy to be ordered under service code number 4822 462 41173

Add 3 capacitors 1n2 and delete 6 capacitors 47p described in mod. level 6 of MOTOR + SEQ module F (see this service information)

Introduced : Module K : mod. level 0
Module L : mod. level 1

Number : D 2

Problem : Colour loss when 2 disc drives operate synchronous and slave drive is in still mode.

Solution : Add resistor 22K between B-TS 7012 and 7B3 on module B.

Connect 9C1 and 7B3 on Module Carrier V.

Introduced : Module B : mod level 8

Number : D 3

Problem : Horizontal distorsion of computer-overlay VP415

Solution : Change C2416 on Video Mix module Y from 8n2 into 100p.

Introduced : Module Y : mod level 5

Number : D 4

Problem : Jitter of computer overlay VP415

Solution : Add resistor 10M parallel to C2415 on Video Mix module Y.

Introduced : Module Y : mod level 6

COMMUNICATION PROBLEMS

Number : E 1

Problem : Disc drive does not accept any commands from ext. computer after printer command <LF><CR> or <CR><LF>.
For instance : LPRINT "F500R"

Solution : -Change mentioned command in :
LPRINT "F500R" ; CHR$(13) ;
-Adaptation of CONTROL software.
(will be released in later stage).

Introduced : -